

**SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE**

DESCRIPTION

The 2SK3114 is N-channel DMOS FET device that features a low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply, AC adapter.

FEATURES

- Low on-state resistance:
 $R_{DS(on)} = 2.2 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 2.0 \text{ A)}$
- Low gate charge:
 $Q_G = 15 \text{ nC TYP. (} V_{DD} = 450 \text{ V, } V_{GS} = 10 \text{ V, } I_D = 4.0 \text{ A)}$
- Gate voltage rating: $\pm 30 \text{ V}$
- Avalanche capability ratings
- Isolated TO-220 package

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	600	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 30	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 4.0	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 16	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	30	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Single Avalanche Current ^{Note2}	I_{AS}	4.0	A
Single Avalanche Energy ^{Note2}	E_{AS}	10.7	mJ

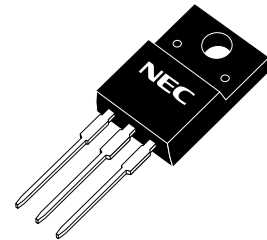
Notes 1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 150 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3114	Isolated TO-220

★ (Isolated TO-220)

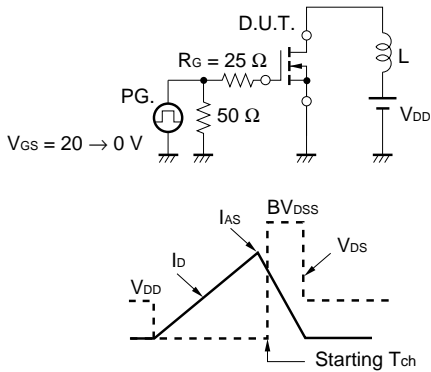


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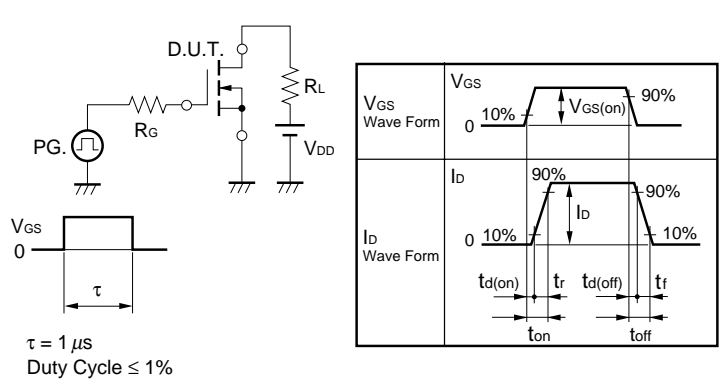
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V			100	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±30 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	2.5		3.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 2.0 A	1.0	50		S
Drain to Source On-state Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 2.0 A		1.6	2.2	Ω
Input Capacitance	C _{iss}	V _{DS} = 10 V		550		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		115		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		13		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 150 V, I _D = 2.0 A		12		ns
Rise Time	t _r	V _{GS(on)} = 10 V		6		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		35		ns
Fall Time	t _f	R _L = 10 Ω		12		ns
Total Gate Charge	Q _G	V _{DD} = 450 V		15		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		4		nC
Gate to Drain Charge	Q _{GD}	I _D = 4.0 A		4.4		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 4.0 A, V _{GS} = 0 V		0.9		V
Reverse Recovery Time	t _{rr}	I _F = 4.0 A, V _{GS} = 0 V		1.3		μs
Reverse Recovery Charge	Q _{rr}	di/dt = 50 A/μs		4.3		μC

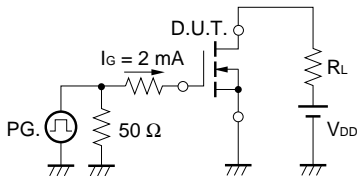
TEST CIRCUIT 1 AVALANCHE CAPABILITY



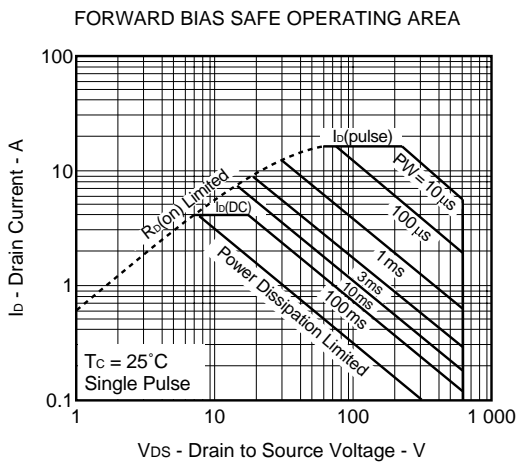
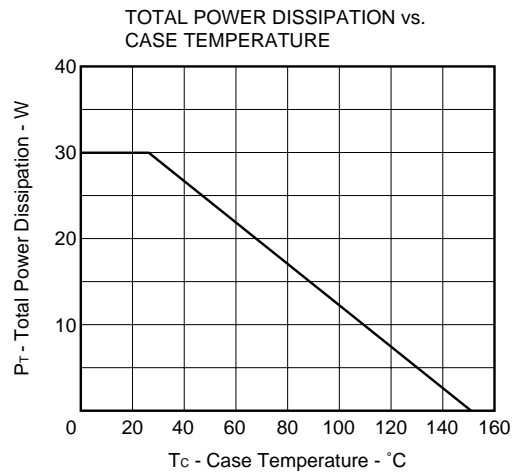
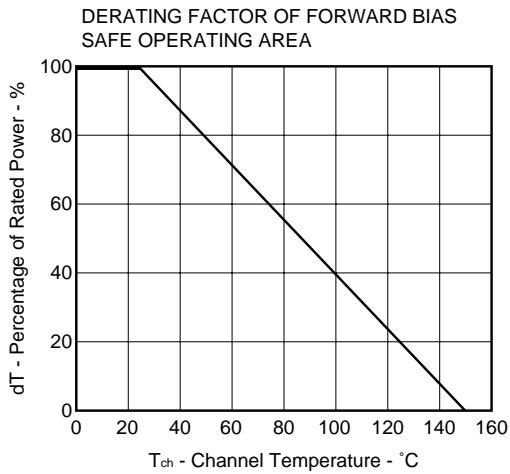
TEST CIRCUIT 2 SWITCHING TIME



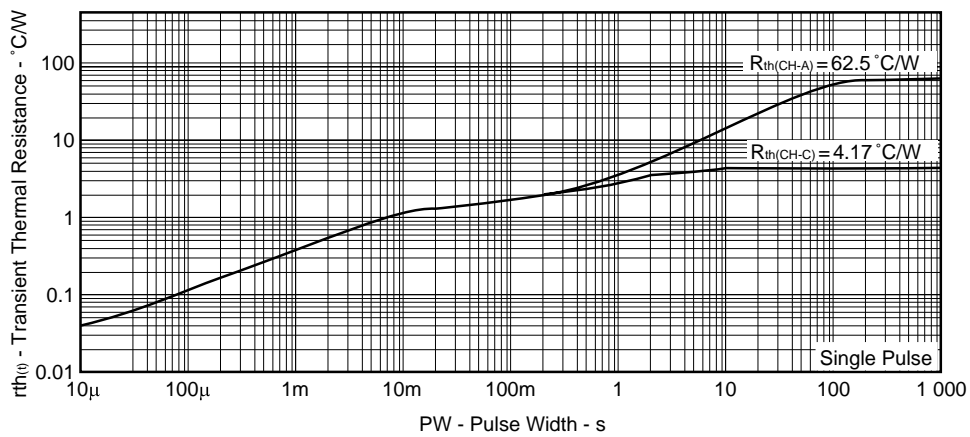
TEST CIRCUIT 3 GATE CHARGE



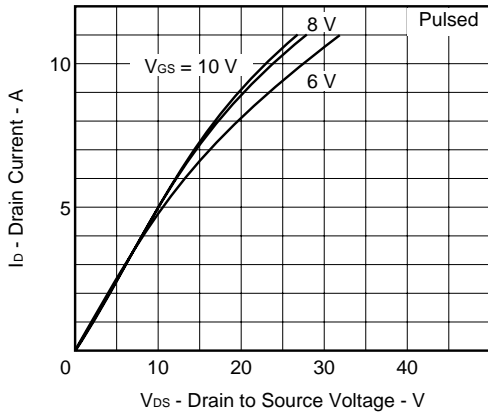
TYPICAL CHARACTERISTICS (T_A = 25°C)



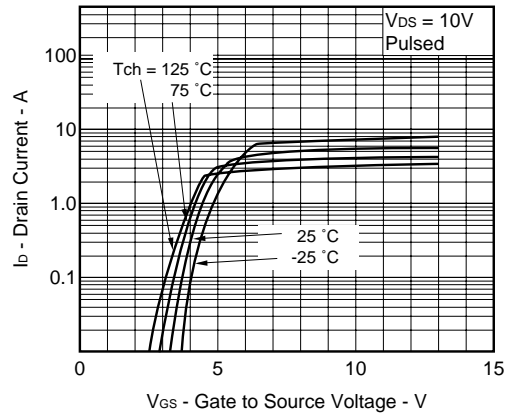
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



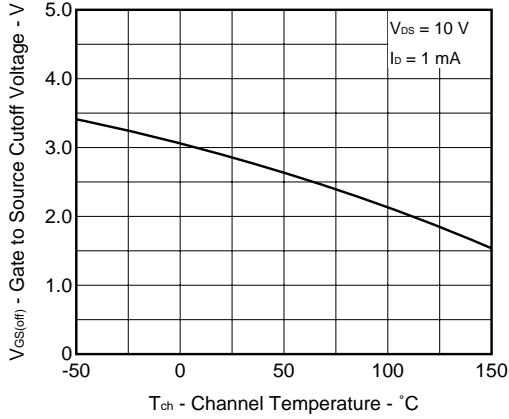
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



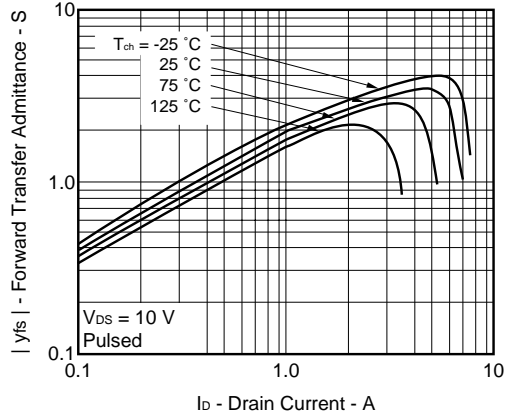
FORWARD TRANSFER CHARACTERISTICS



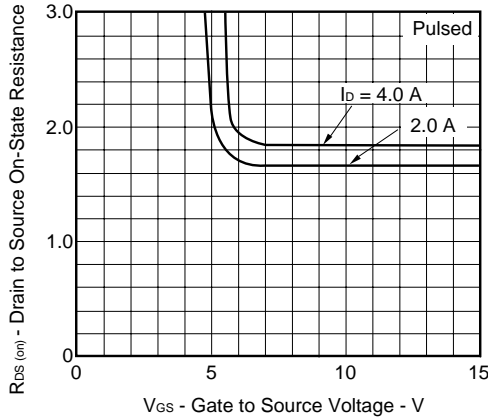
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



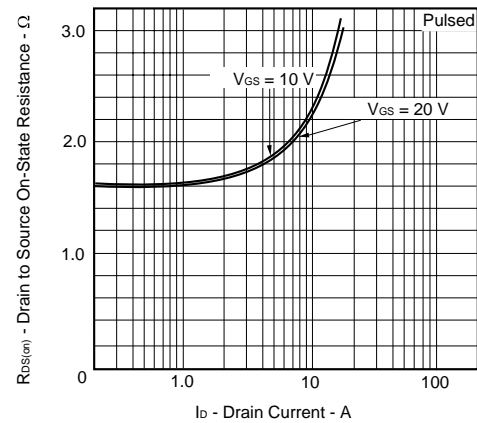
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

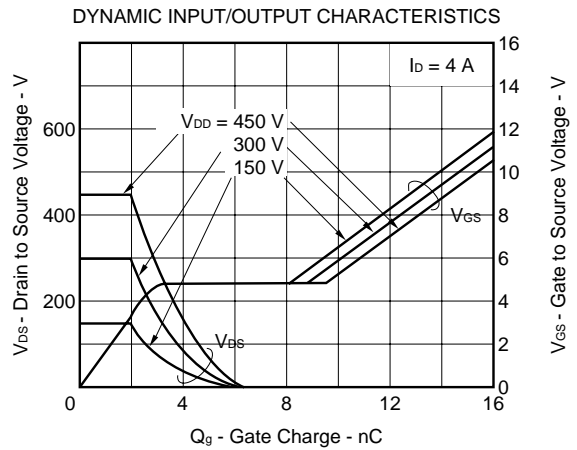
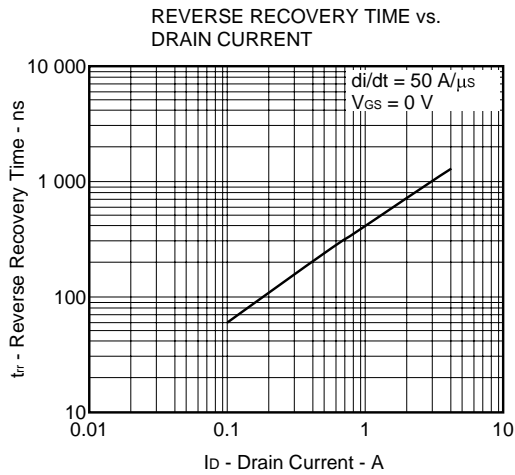
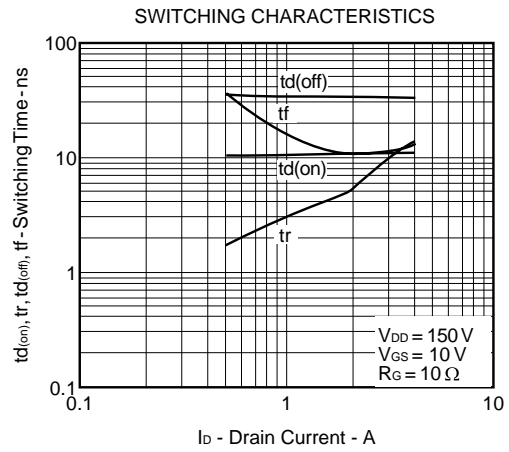
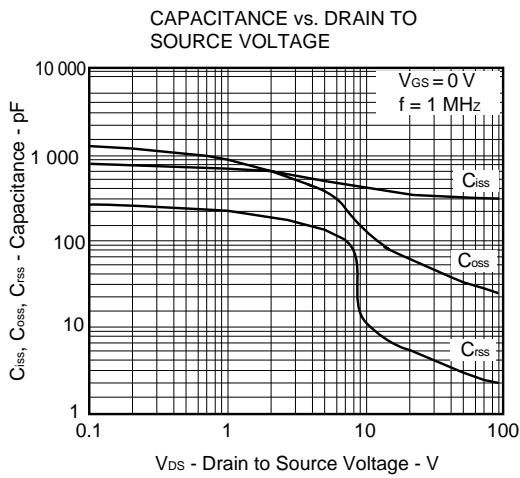
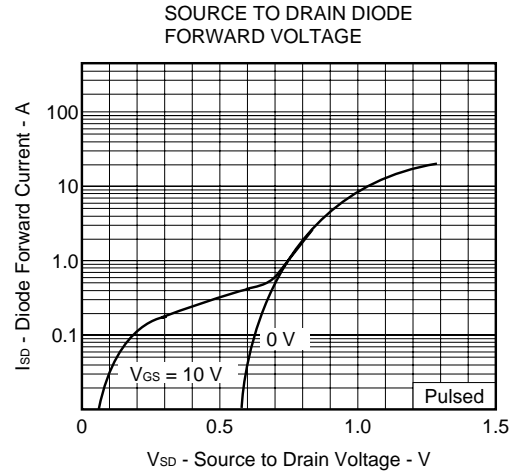
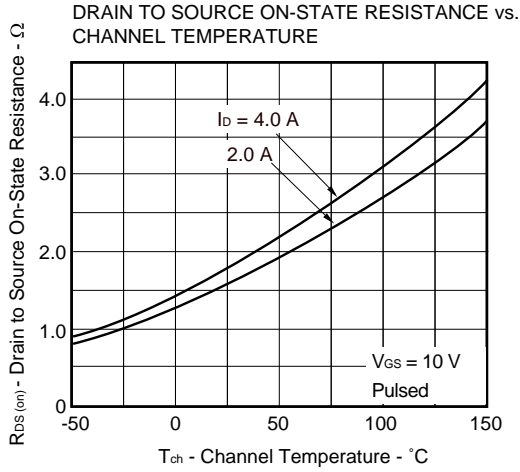


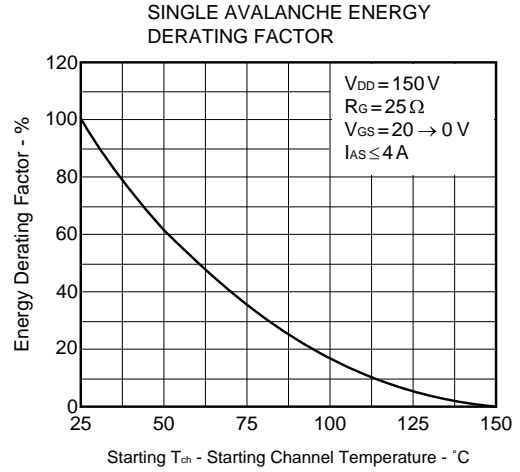
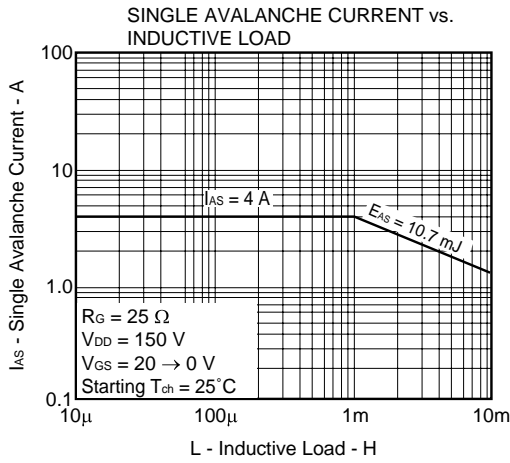
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



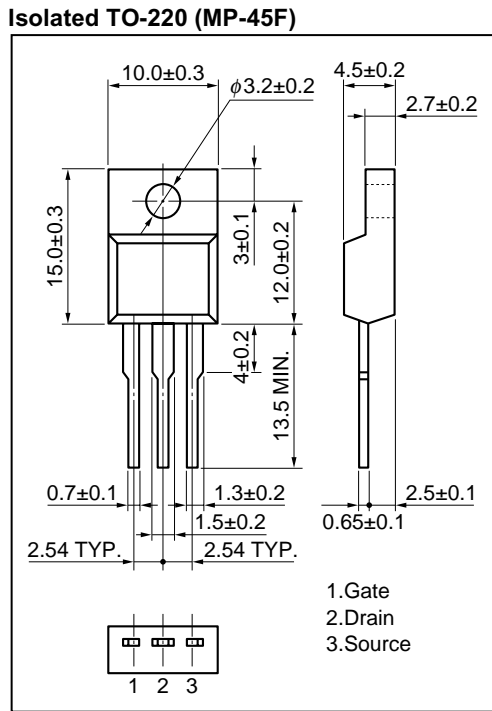
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



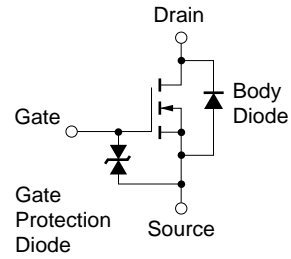




PACKAGE DRAWINGS (Unit: mm)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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