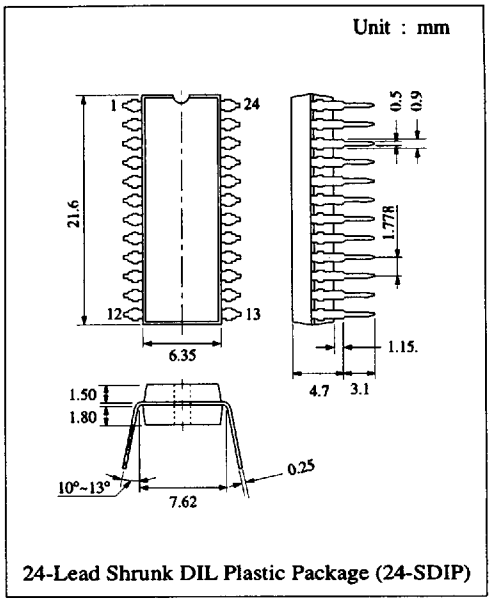
AN7348K

Dual Record/Playback Pre-Amplifier IC for Double Cassette



24-Lead Shrunk DIL Plastic Package (24-SDIP)

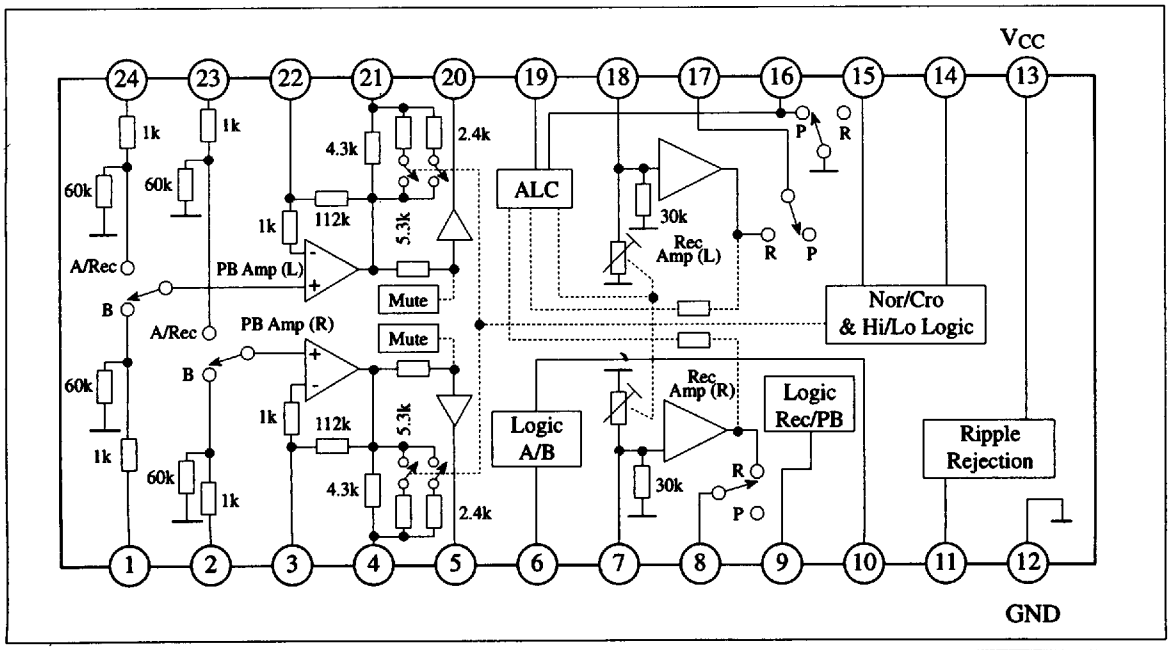
■ Description

The AN7348K is a monolithic integrated circuit designed for double cassette recorder. It has dual channel PB / Rec amplifier with ALC function. Tape A (PB only) and Tape B (PB / Rec) select, Normal / Chrome select, Normal / High speed dubbing select and Rec / PB selection are easily controlled by 4 pins. It requires no external FET switches at PB amp. input and Rec amp. output. External components are also minimized. In addition, this IC has low susceptibility to EMC.

■ Features

- Built-in Normal / Chrome equalizier for PB amplifier
- Built-in Normal / High speed equalization for PB amplifier
- Built-in Tape A/B switching
- Built-in Rec / PB select
- ALC function for recording
- Wide operating supply voltage range : Vcc = 3.6V ~ 12V
- Can connect IC directly to tape head. No external FET switches is required
- Minimum switching noise.

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	12.4	V
Supply Current	I_{CC}	40	mA
Power Dissipation	P_D	500	mW
Operating Ambient Temperature	Topr	-20 ~ +75	°C
Storage Temperature	Tstg	-55 ~ +150	°C

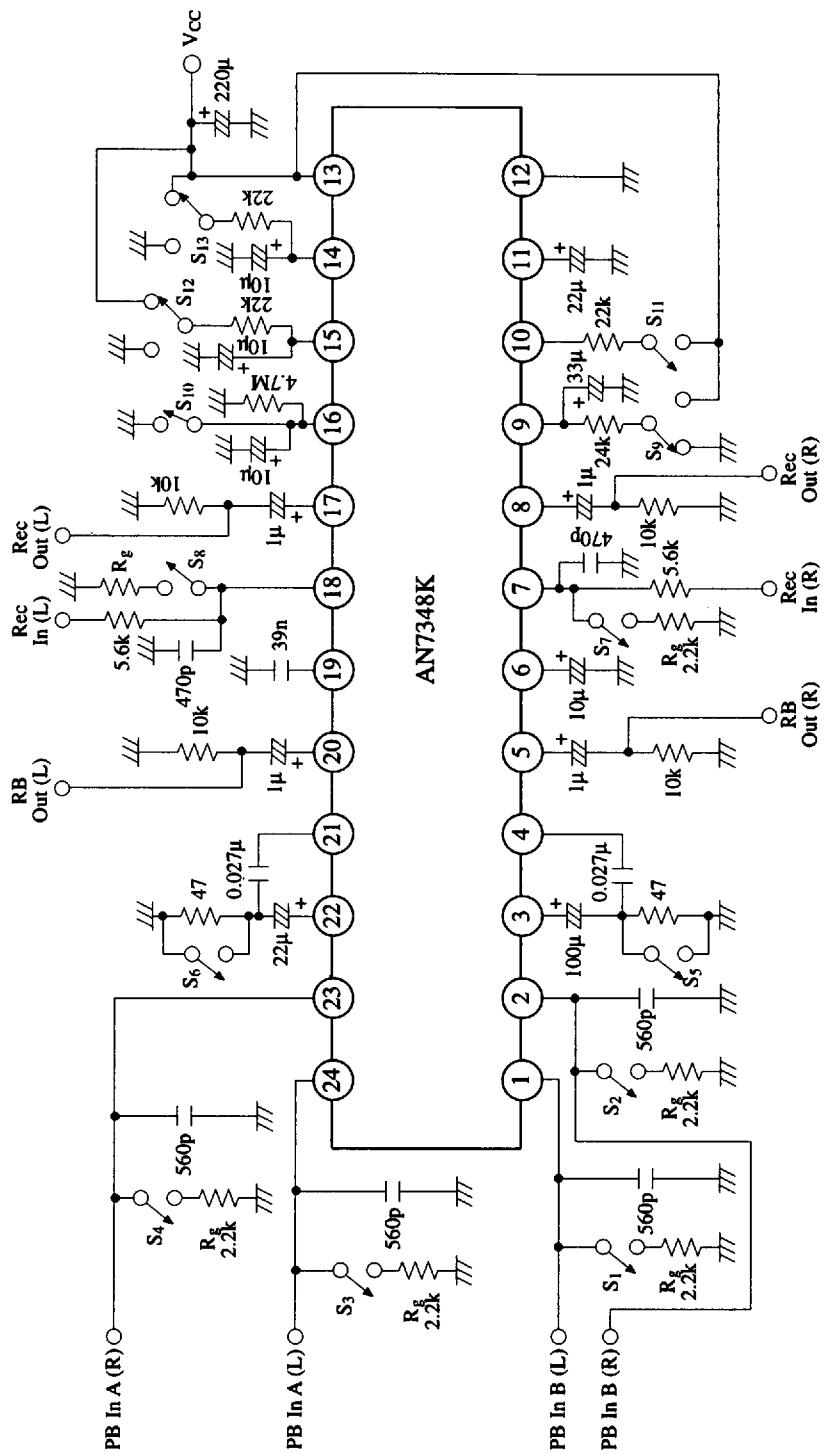
Operating Supply Voltage Range: V_{CC} = 3.6V ~ 12.0V

■ Electrical Characteristics (V_{CC}=5V, Ta=25°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
Quiescent Circuit Current (REC)	I_{CQrec}	V_{in} = 0V	12.0	18	24	mA
Playback Amplifier						
Close Loop Gain	$G_{VC(P)}$	V_{in} = 5.6mVrms	40	42.5	45	dB
Open-Loop Gain	$G_{VO(P)}$	V_{in} = 89μVrms	75	81		dB
Input Noise	$V_{ni(p)}$	R_g = 2.2kΩ, DIN/AUDIO, V_{in} = V_{no} / G_{VC}		1.8	2.5	μV
Total Harmonic Distortion	$THD_{(P)}$	V_O = 1Vrms, BPF		0.05	0.1	%
Max. Output Voltage	$V_{O(P)}$	THD = 3%, BPF	1.4	1.7		Vrms
Channel Balance	$CB_{(P)}$	V_{in} = 5.6mVrms	-1.5	0	1.5	dB
Channel Crosstalk	$CT_{C(P)}$	V_{in} = 5.6mVrms, R_g = 2.2kΩ, DIN/AUDIO	55	65		dB
Source Crosstalk	$CT_{S(P)}$	V_{in} = 5.6mVrms, R_g = 2.2kΩ, DIN/AUDIO	55	65		dB
Playback EQ						
120μs / 70μs ΔGain *1	ΔG_{vc1}	V_{in}=10mVrms, f=10kHz	4	4.6	5.2	dB
1x / 2x Dubbing ΔGain*2	ΔG_{vc2}	V_{in}=22mVrms, f=10kHz	4	4.6	5.2	dB
Record Amplifier ALC OFF						
Output Noise Voltage	$V_{no(R)}$	R_g=1.0kΩ, DIN Audio		220	550	μV
Closed-Loop Gain	$G_{VC(R)}$	V_{in}=12mVrms	35.5	38.5	42	dB
Total Harmonic Distortion	$THD_{(R)}$	V_o=1.0Vrms, BPF		0.05	0.17	%
Max. Output Voltage	$V_{O(R)}$	THD=3%, BPF	1.4	1.8		V
Channel Crosstalk	$CT_{C(R)}$	V_{in}=8mVrms, R_g=1.0kΩ,Din Audio	55	66		dB
ALC (2 Channel Input) ALC ON						
ALC Voltage	V_{ALC}	R_{ext}=5.6kΩ, Dual i/p, V_{in}=12mVrms	0.75	1.0	1.37	Vrms
ALC Range	W_{ALC}	R_{ext}=5.6kΩ, from V_{in}=10mV to Vo=+3dB	35	51		dB
ALC Channel Balance	$CB_{(ALC)}$	R_{ext}=5.6kΩ, V_{in}=12mVrms	-2	0	2	dB
Playback Mode						
PB to Rec Crosstalk*3	$CT_{R/P}$	Vin=12mVrms at Rec i/p, measure at Rec o/p	70	88		dB

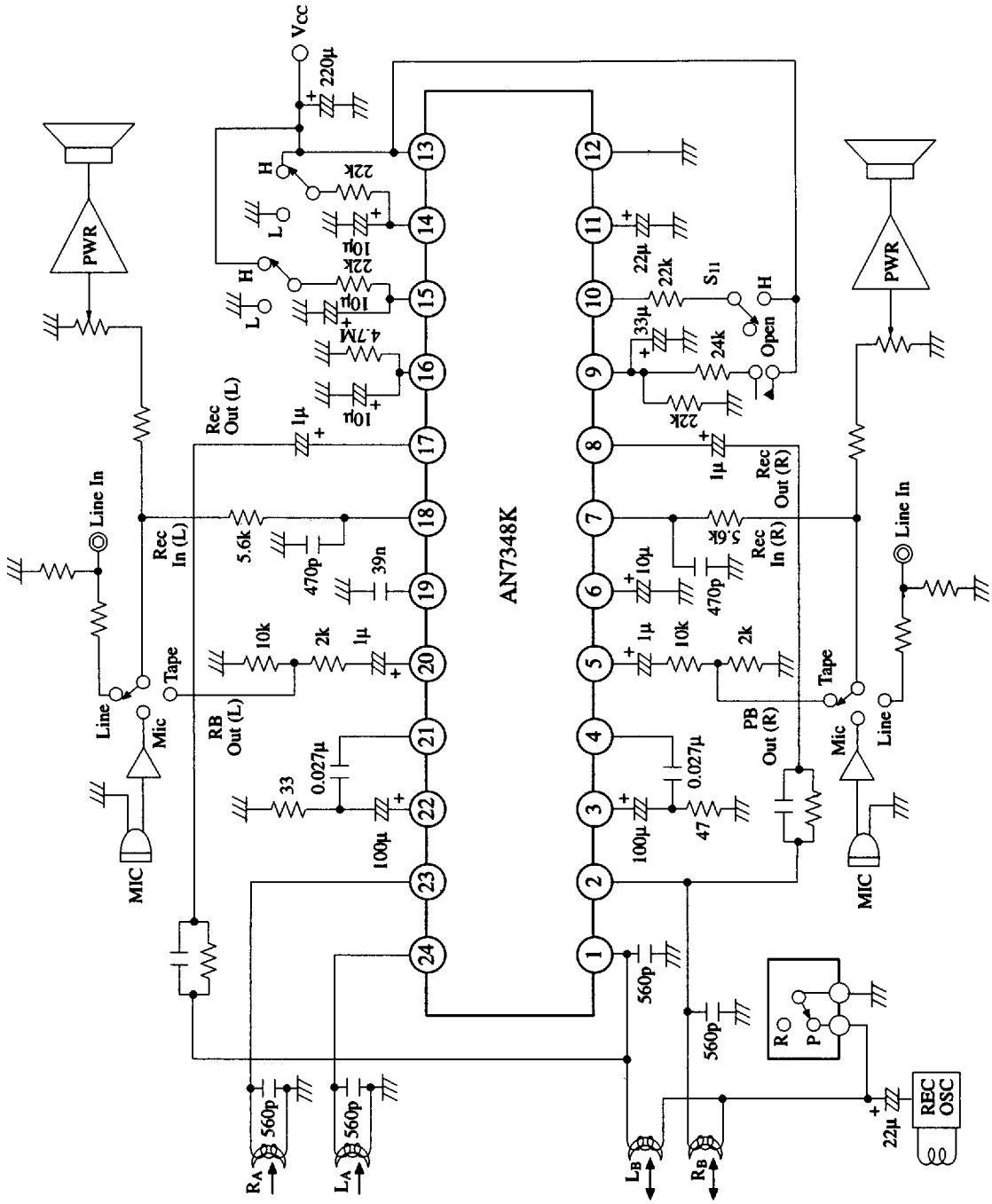
Note : *1 ΔG_{vc1} = (G_{vc} at 120μs) - (G_{vc} at 70μs)
*2 ΔG_{vc2} = (G_{vc} at 1 x) - (G_{vc} at 2 x)
*3 $CT_{R/P}$ = 20log(Vb (PB mode) + Vb (REC mode))

■ Test Circuit



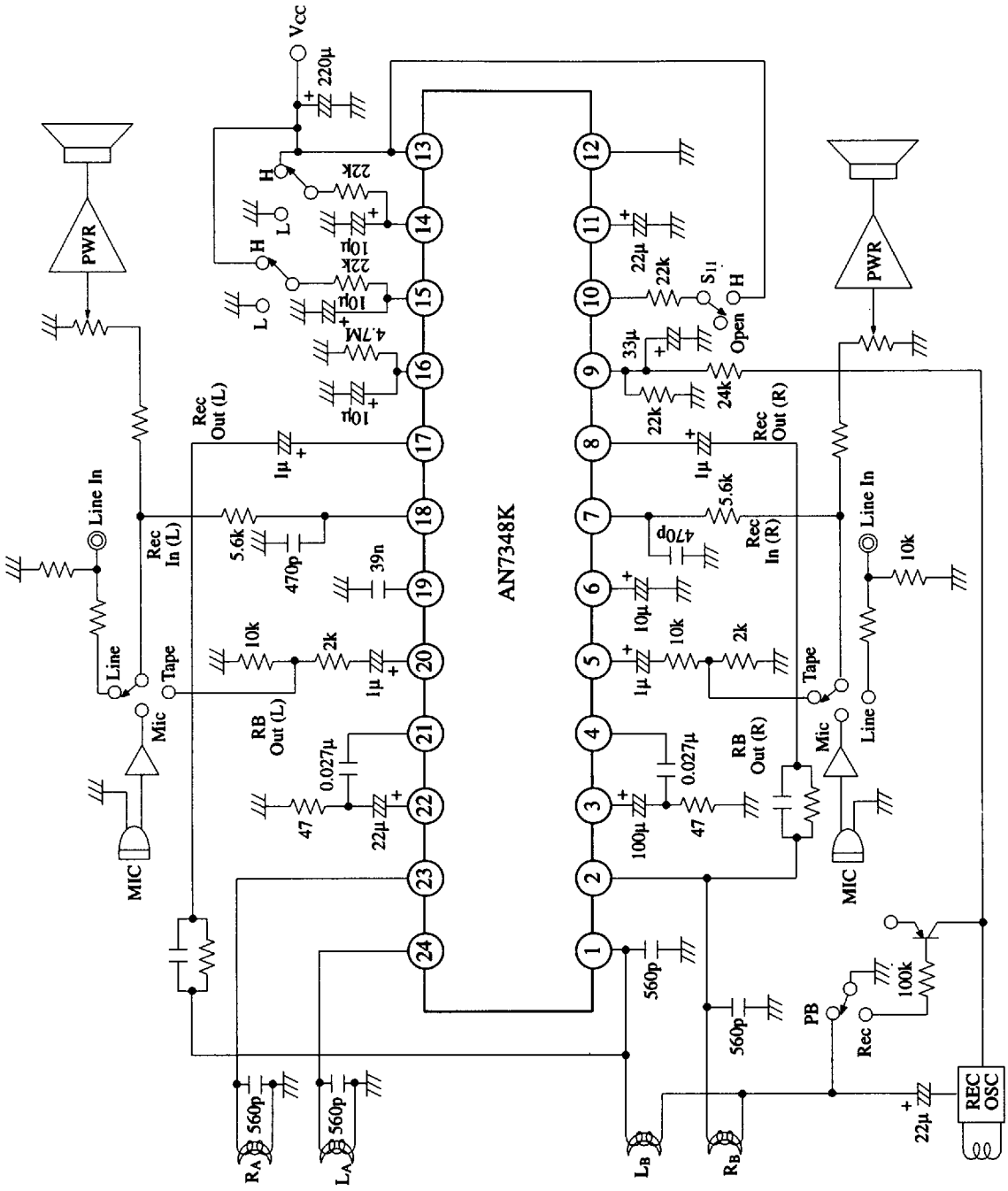
Switch / Logic	A/B (S_{11})	Rec / PB (S_9)	Nor / Cro (S_{13})	Hi / Lo (S_{12})
High	Tape A	Rec	Chrome	2 x speed
Open	Tape B	PB	Normal	1 x speed
Low	Tape B	PB	Normal	1 x speed

■ Application Circuit - Logic Deck



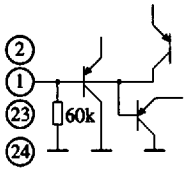
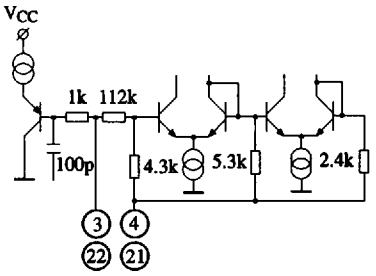
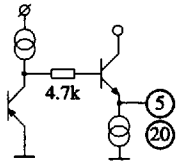
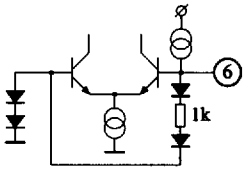
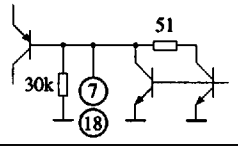
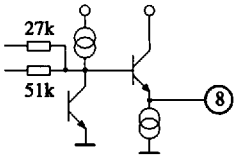
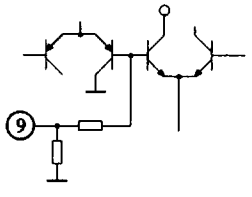
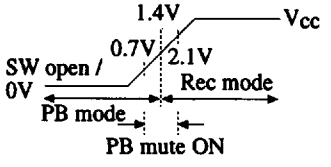
Pin / Logic	A/B (P10)	Rec / PB (P9)	Nor / Cro (P14)	Hi / Lo (P15)
High	Tape A	Rec	Chrome	2 x speed
Open	Tape B	PB	Normal	1 x speed
Low	Tape B	PB	Normal	1 x speed

■ Application Circuit 2

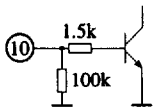
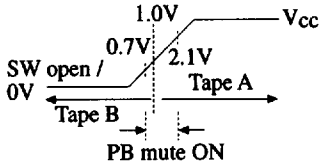
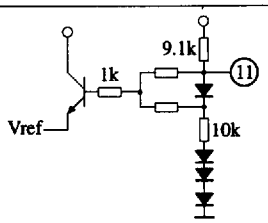
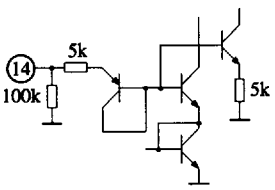
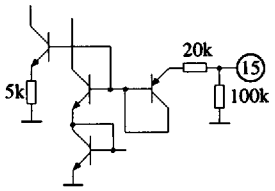
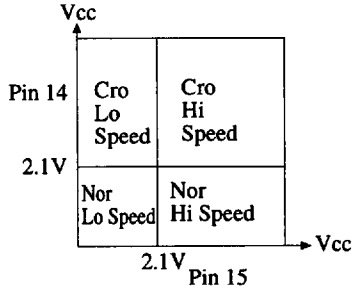
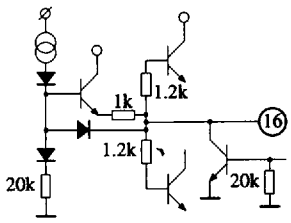
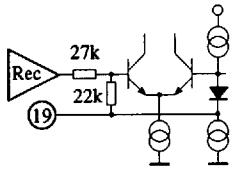


Pin / Logic	A/B (P10)	Rec / PB (P9)	Nor / Cro (P14)	Hi / Lo (P15)
High	Tape A	Rec	Chrome	2 x speed
Open	Tape B	PB	Normal	1 x speed
Low	Tape B	PB	Normal	1 x speed

■ Pin Descriptions

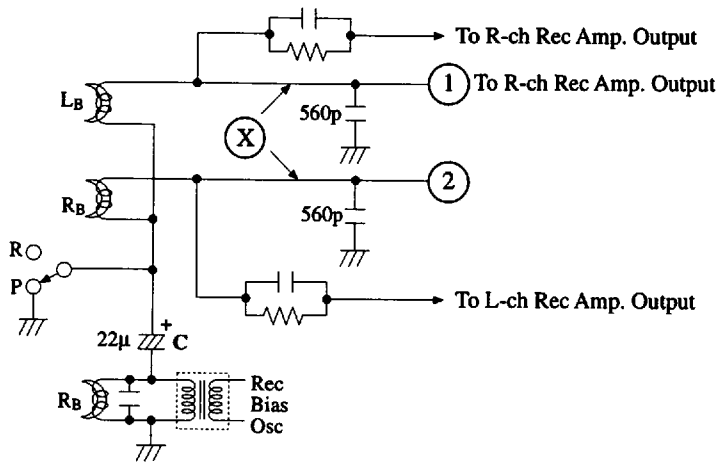
Pin No.	Pin Name	Equivalent Circuit	Description
1	L-ch Playback Amp. Input (B)		Playback amp. input Input impedance = 61kΩ Pin 1, 2, 23 & 24 = 0V (PB mode) *Pin 1, 2 = 2.1V (Rec mode) *Pin 23, 24 = 0V (Rec mode)
2	R-ch Playback Amp. Input (B)		
23	R-ch Playback Amp. Input (A)		
24	L-ch Playback Amp. Input (A)		
3	R-ch Playback Negative Feedback		Playback amp. feedback loop DC = 0.7V.
22	L-ch Playback Negative Feedback		
4	R-ch Playback Equalization		Playback equalization for both Normal / Chrome and High / Low dubbing
21	L-ch Playback Equalization		
5	R-ch Playback Amp Output		Low output impedance
20	L-ch Playback Amp Output		
6	AB Switch τ		Determines the tape A/B switching time constant with an external capacitor DC : 2.8V (pin 10 high) DC : 0.0V (pin 10 open)
7	R-ch Rec Input		Rec amp input pin Input impedance = 30kΩ
18	L-ch Rec Input		
8	R-ch Rec Output		Rec amp output pin DC = Vref, Zout = Low (pin 9 High) DC = =V, Zout = High (pin 9 Open)
17	L-ch Rec Output		
9	Rec / Playback Switch		Select Rec or playback mode 0.7V > Threshold > 2.1V 

■ Pin Descriptions (Continue)

Pin No.	Pin Name	Equivalent Circuit	Description
10	AB Switch		To select Tape A or Tape B 0.7V > Threshold > 2.1V 
11	Ripple Filter		Connect with a capacitor to minimize ripple from Vcc DC = 4.4V (Vcc = 6V)
12	GND		
13	Vcc		
14	Chrome / Normal		Input to control Playback EQ for Chrome or Normal Tape
15	Hi / Lo		Input to control Playback EQ for High or Low dubbing 
16	ALC τ		Controls the attack and release time of ALC DC = 1.4V → Rec mode DC = 0V → Playback mode
19	ALC Low Cut		ALC comparator circuit reference voltage

■ Supplementary Explanation

1) Recording mode

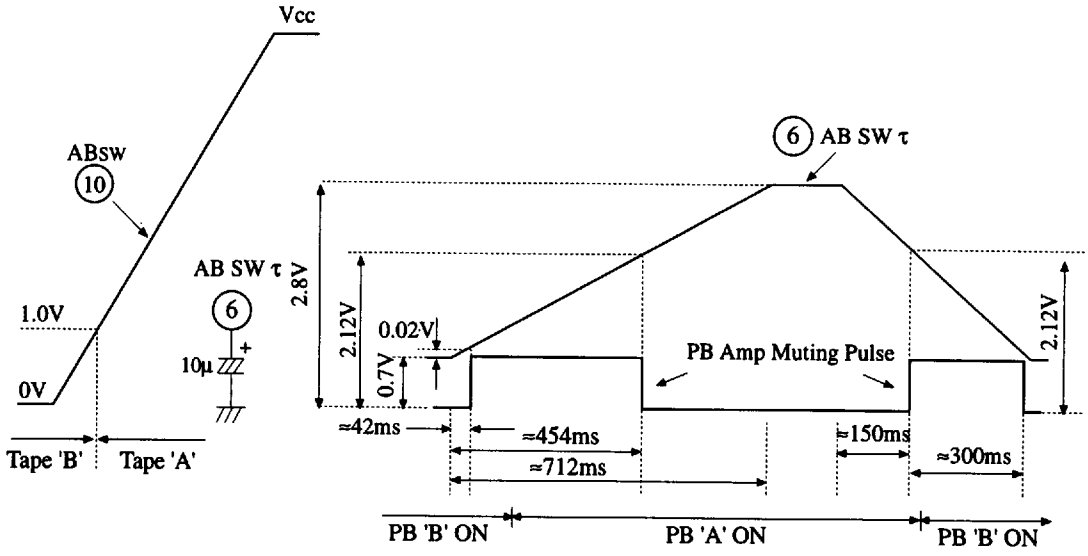


During dubbing mode, Sw1 will be in Rec position and point X will be bias at 2.1V internally (Vcc = 6V). This is to ensure enough dynamic swing for the recording signal. Capacitor C is therefore necessary to couple the dc bias at point X to Rec bias oscillator. When in playback mode, point X will return to 0V and Sw1 is switch to PB position. Capacitor C should be chosen carefully to avoid degradation of the Rec bias Osc.signal & recording signal. The recommended value is 22μF.

2) ALC Detector

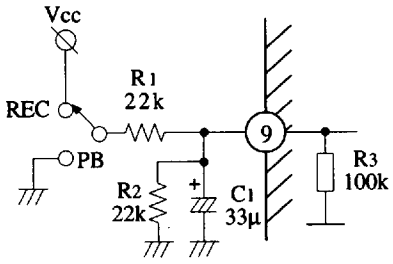
The ALC circuit will be cut off during playback mode. This is achieved internally in the IC by shorting pin 16 to ground. By chosing different values of R, C combination at pin 16, the ALC attack and release time can be varied.

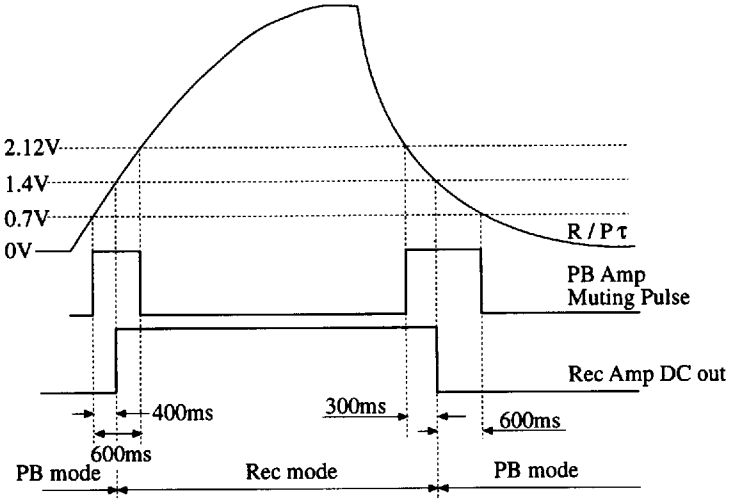
3) A / B Switch muting



■ Supplementary Explanation (Continue)

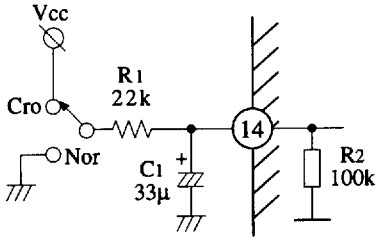
4) R / PB Switching muting
(A/B sw = 'B' mode)

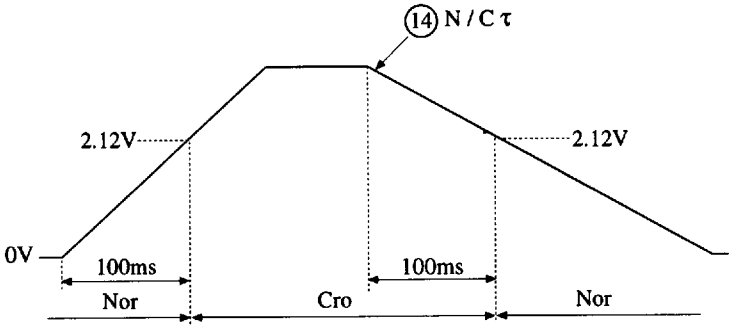




Charging $\tau \approx R1*C1$
Discharging $\tau \approx (R2//R3)*C1$
0.7V > Threshold Voltage > 2.1V

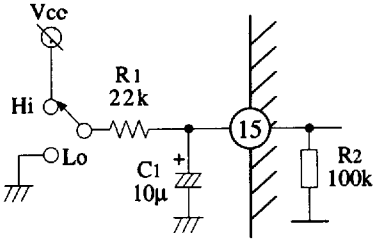
5) Nor / Cro Switching

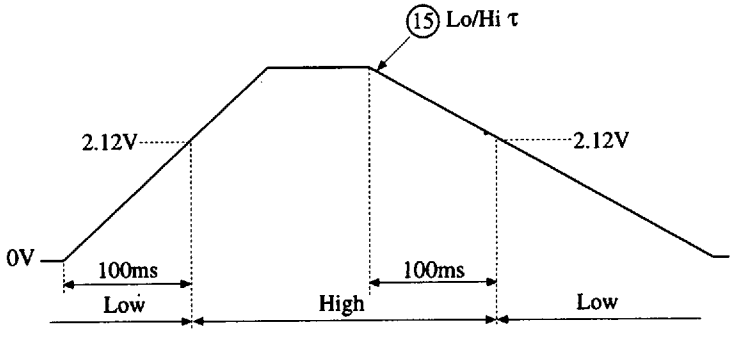




Charging $\tau \approx R1*C1$
Discharging $\tau \approx (R1//R2)*C1$

6) I o / Hi Dubbing Switching



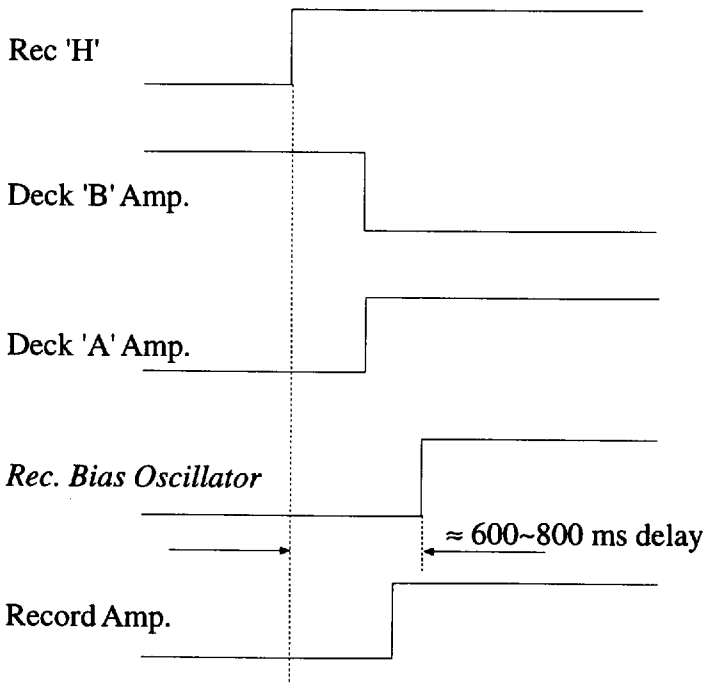


Charging $\tau \approx R1*C1$
Discharging $\tau \approx (R1//R2)*C1$

■ Supplementary Explanation (Continue)

7) Rec 'H' swiching

When the Rec/PB switch (pin 9) is switched to record mode, the pre-amp will switch from deck 'B' to deck 'A' mode (if the ABsw, pin 10 is low). The pre-amp switching τ is govern by the capacitor at pin 6. Therefore it is necessary to delay the turning ON time of the record bias oscillator circuit. This is to prevent any switching noise from the oscillator circuit from leaking through the 'B' amp during the initial switching period. The prefer switching sequence is shown below.



8) PCB layout for Pre -amp INPUTs.

To prevent oscillation, the input paths for pin 1 & 2 should avoid crossing or running next to the input paths for pin 23 & 24. This will also ensure minimun source leakage especially during record mode.

■ Printed Circuit Board Layout (Scale 1:1)