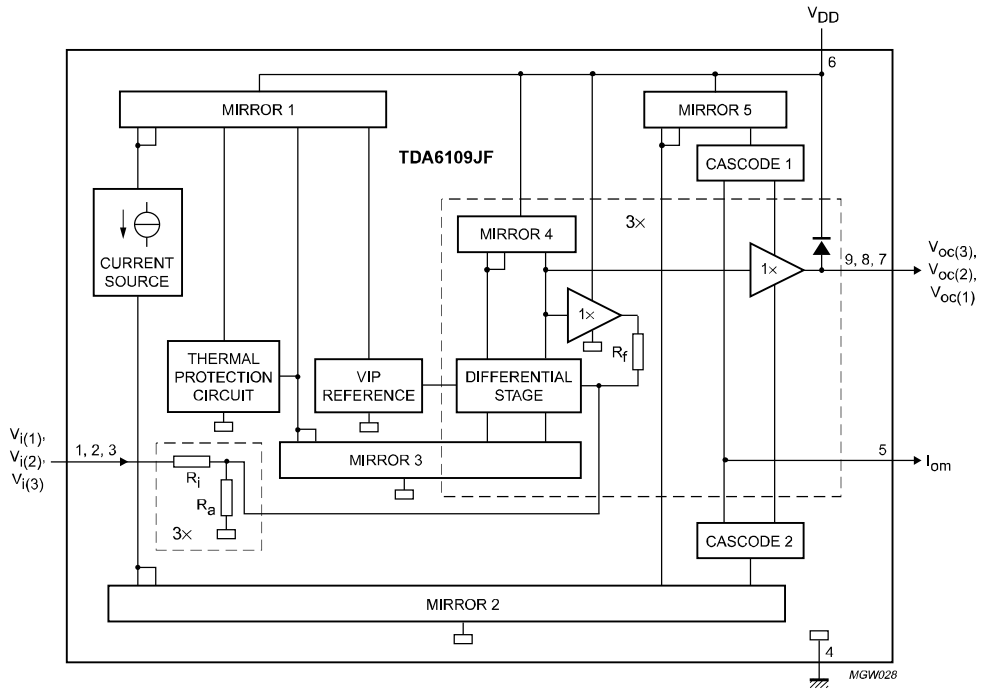
TDA6109JF (IC1801)

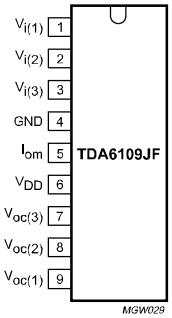
Block Diagram



Block diagram (one amplifier shown).

Pinning

SYMBOL	PIN	DESCRIPTION
$V_{i(1)}$	1	inverting input 1
$V_{i(2)}$	2	inverting input 2
$V_{i(3)}$	3	inverting input 3
GND	4	ground (fin)
I_{om}	5	black current measurement output
V_{DD}	6	supply voltage
$V_{oc(3)}$	7	cathode output 3
$V_{oc(2)}$	8	cathode output 2
$V_{oc(1)}$	9	cathode output 1



Pin configuration.

Limiting Values

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages measured with respect to pin 4 (ground); currents as specified in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		0	250	V
V_i	input voltage		0	12	V
V_{om}	measurement output voltage		0	6	V
V_{oc}	cathode output voltage		0	V_{DD}	V
$\lvert I_{om(mean)} \rvert$	absolute value of mean current of measurement output (for three channels)	1.5 V < V_i < 5.5 V; 3 V < V_{om} < 6 V	–	5	mA
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–20	+150	°C
V_{es}	electrostatic handling				
	human body model (HBM)		–	2000	V
	machine model (MM)		–	300	V

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Characteristics

Operating range: T_j = –20 to +150 °C; V_{DD} = 180 to 210 V. Test conditions: T_{amb} = 25 °C; V_{DD} = 200 V; $V_{oc(1)} = V_{oc(2)} = V_{oc(3)} = \frac{1}{2}V_{DD}$; C_L = 10 pF (C_L consists of parasitic and cathode capacitance); $R_{th(h-a)}$ = 18 K/W (measured in test circuit of Fig.8); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_q	quiescent supply current		8.8	10.3	11.7	mA
$V_{ref(int)}$	internal reference voltage (input stage)		–	2.5	–	V
R_i	input resistance		–	3.2	–	kΩ
G	gain of amplifier		47.5	51.0	55.0	
ΔG	gain difference		–2.5	0	+2.5	
V_{oc}	nominal output voltage at pins 7, 8 and 9 (DC value)	I_i = 0 μA	116	129	142	V
$\Delta V_{oc(offset)}$	differential nominal output offset voltage between pins 7 and 8, 8 and 9 and 9 and 7 (DC value)	I_i = 0 μA	–	0	5	V
$\Delta V_{oc(T)}$	output voltage temperature drift at pins 7, 8 and 9		–	–10	–	mV/K
$\Delta V_{oc(offset)(T)}$	differential output offset voltage temperature drift between pins 7 and 8, 8 and 9 and 7 and 9		–	0	–	mV/K
$I_{om(offset)}$	offset current of measurement output (for three channels)	I_{oc} = 0 μA; 1.5 V < V_i < 5.5 V; 3 V < V_{om} < 6 V	–50	–	+50	μA
$\Delta I_{om}/\Delta I_{oc}$	linearity of current transfer (for three channels)	–100 μA < I_{oc} < 100 μA; 1.5 V < V_i < 5.5 V; 3 V < V_{om} < 6 V	0.9	1.0	1.1	
		–100 μA < I_{oc} < 18 mA; 1.5 V < V_i < 5.5 V; 3 V < V_{om} < 4 V	0.9	1.0	1.1	
$I_{oc(max)}$	maximum peak output current (pins 7, 8 and 9)	50 V < V_{oc} < V_{DD} – 50 V	–	28	–	mA
$V_{oc(min)}$	minimum output voltage (pins 7, 8 and 9)	V_i = 7.0 V; note 1	–	–	10	V
$V_{oc(max)}$	maximum output voltage (pins 7, 8 and 9)	V_i = 1.0 V; note 1	V_{DD} – 15	–	–	V
B_S	small signal bandwidth (pins 7, 8 and 9)	V_{oc} = 60 V (p-p)	–	9.0	–	MHz
B_L	large signal bandwidth (pins 7, 8 and 9)	V_{oc} = 100 V (p-p)	–	8.0	–	MHz
$t_{P(oc)}$	cathode output propagation time 50% input to 50% output (pins 7, 8 and 9)	V_{oc} = 100 V (p-p) square wave; f <1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3); see Figs 6 and 7	–	32	–	ns
$\Delta t_{P(oc)}$	difference in cathode output propagation time 50% input to 50% output (pins 7 and 8, 7 and 9 and 8 and 9)	V_{oc} = 100 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3)	–10	0	+10	ns

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Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{r(oc)}$	cathode output rise time 10% output to 90% output (pins 7, 8 and 9)	V_{oc} = 50 to 150 V square wave; f < 1 MHz; t_f = 40 ns (pins 1, 2 and 3); see Fig.6	35	50	65	ns
$t_{f(oc)}$	cathode output fall time 90% output to 10% output (pins 7, 8 and 9)	V_{oc} = 150 to 50 V square wave; f < 1 MHz; t_r = 40 ns (pins 1, 2 and 3); see Fig.7	35	50	65	ns
t_{st}	settling time 50% input to 99% < output < 101% (pins 7, 8 and 9)	V_{oc} = 100 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3); see Figs 6 and 7	–	–	350	ns
SR	slew rate between 50 V to (V_{DD} – 50 V) (pins 7, 8 and 9)	V_i = 4 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3)	–	1850	–	V/µs
$V_{oc(overshoot)}$	cathode output voltage overshoot (pins 7, 8 and 9)	V_{oc} = 100 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3); see Figs 6 and 7	–	10	–	%
PSRR	power supply rejection ratio	f < 50 kHz; note 2	–	65	–	dB
$\alpha_{ct(DC)}$	DC crosstalk between channels		–	–50	–	dB

Notes

1. See also Fig.5 for the typical DC-to-DC transfer of V_i to V_{oc}.
2. The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.