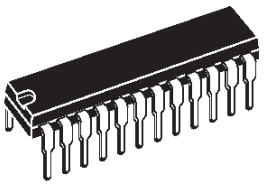
TDA9203A

I²C BUS CONTROLLED 70MHz RGB PREAMPLIFIER

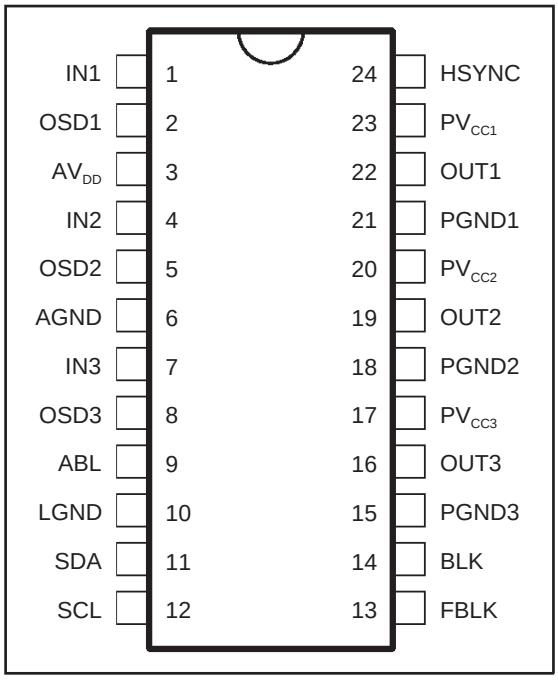
- 70MHz TYPICAL BANDWIDTH AT 4V_{PP} OUTPUT WITH 12pF CAPACITIVE LOAD
- 5.5ns TYPICAL RISE/FALL TIME AT 4V_{PP} OUTPUT WITH 12pF CAPACITIVE LOAD
- POWERFULL OUTPUT DRIVE CAPABILITY
- BRT, CONT, DRIVE, OUTPUT DC LEVEL, OSD CONTRAST, BACK-PORCH CLAMPING PULSE WIDTH ARE I²C BUS CONTROLLED
- INTERNAL BACK-PORCH CLAMPING PULSE GENERATOR
- OSD WHITE BALANCE TRACKING
- INTERNAL OSD SWITCHES
- BLANKING AND FAST-BLANKING INPUTS
- VERY LARGE DRIVE ADJUSTMENT RANGE (48dB)
- SEMI-TRANSPARENT BACKGROUND ON OSD PICTURE
- ABL CONTROL



SHRINK 24
(Plastic Package)

ORDER CODE : TDA9203A

PIN CONNECTIONS



9203A-01.EPS

DESCRIPTION

The TDA9203A is a digitaly controlled wideband video preamplifier intended for use in mid range color monitor. All controls and adjustments are digitaly performed thanks to I²C serial bus. Contrast, brightness and DC output level of RGB signals are common to the 3 channels and drive adjustment is separate for each channel. Three I²C gain controlled OSD inputs can be switched with RGB signals using fast blanking command. Clamping of RGB signals is performed thanks to a flexible integrated system. The white balance adjustment is effective on brightness, video and OSD signals. The TDA9203A works for application using AC or DC coupled CRT driver.

The ABL input provides a 12dB Max. attenuation on the current contrast value according average beam limitation voltage.

Because of its features and due to component saving the TDA9203A leads to a very performant and cost effective application.

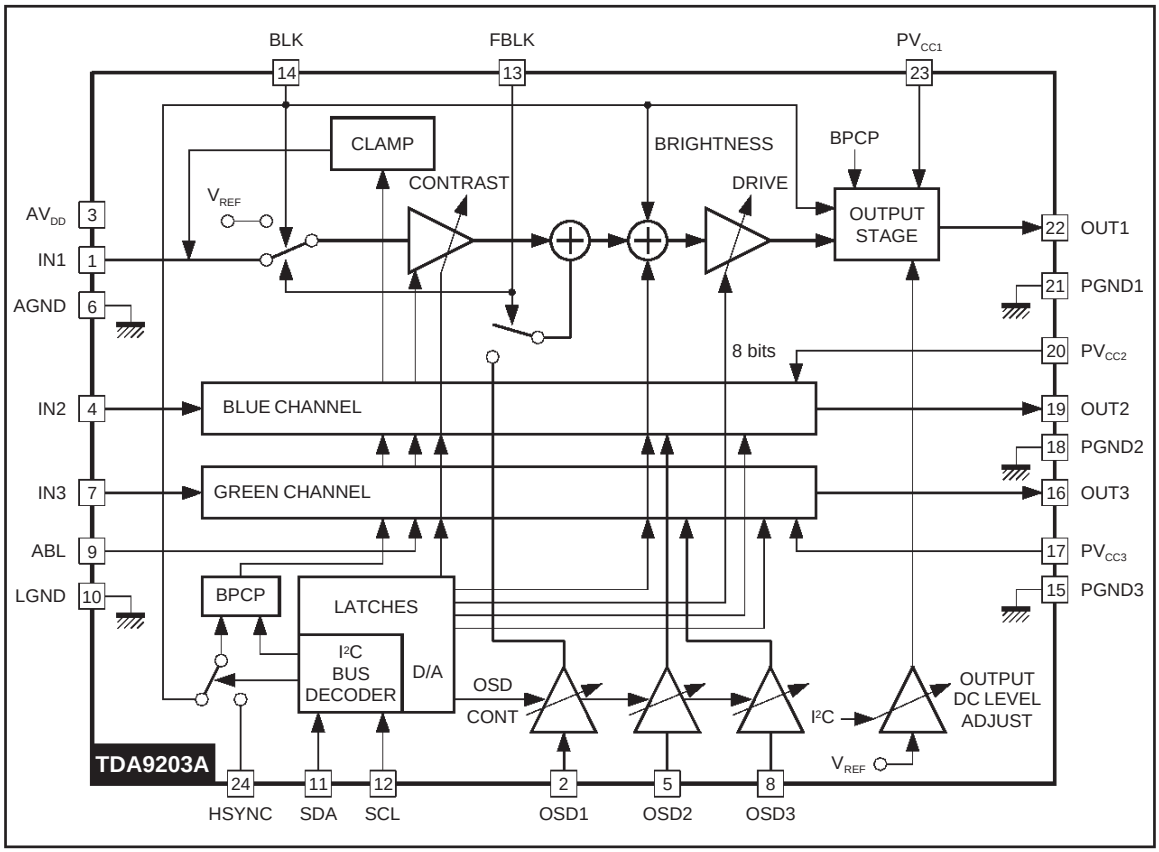
PIN DESCRIPTION

Name	Pin	Type	Function
IN1	1	I	1st Channel Main Picture Input
OSD1	2	I	1st Channel OSD Input
AV_{DD}	3	I	12V Analog V_{DD}
IN2	4	I	2nd Channel Main Picture Input
OSD2	5	I	2nd Channel OSD Input
AGND	6	I/O	Analog Ground
IN3	7	I	3rd Channel Main Picture Input
OSD3	8	I	3rd Channel OSD Input
ABL	9	I	ABL Input
LGND	10	I/O	Logic Ground
SDA	11	I/O	Serial Data Line
SCL	12	I	Serial Clock Line

Name	Pin	Type	Function
FBLK	13	I	Fast Blanking Input
BLK	14	I	Blanking Input
PGND3	15	I/O	3rd Channel Power Ground
OUT3	16	O	3rd Channel Output
PV_{CC3}	17	I	3rd Channel Power V_{CC}
PGND2	18	I/O	2nd Channel Power Ground
OUT2	19	O	2nd Channel Output
PV_{CC2}	20	I	2nd Channel Power V_{CC}
PGND1	21	I/O	1st Channel Power Ground
OUT1	22	O	1st Channel Output
PV_{CC1}	23	I	1st Channel Power V_{CC}
HSYNC	24	I	Horizontal Synch Input

9203A-01.TBL

BLOCK DIAGRAM



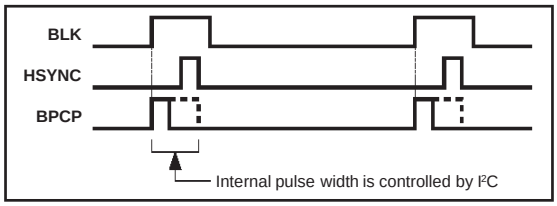
9203A-02.EPS

FUNCTIONAL DESCRIPTION

Input Stage

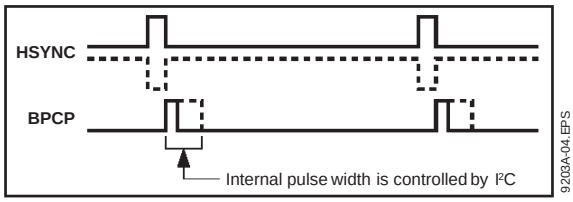
The R, G and B signals must be fed to the three inputs through coupling capacitors (100nF).
The maximum input peak-to-peak video amplitude is 1V.
The input stage includes a clamping function. This clamp is using the input serial capacitor as "memory capacitor" and is gated by an internally generated "Back-Porch-Clamping-Pulse (BPCP)".
The synchronization edge of the BPCP is selected according bit 0 of register R8.
When B0R8 is set to 1, the BPCP is synchronized on the leading edge of the blanking pulse BLK inputs on Pin 14 (see Figure 1). B7R8 allows to use positive or negative blanking signal on Pin 14. At power on reset TDA9203A use only positive blanking.

Figure 1



When B0R8 is clear to 0, the BPCP is synchronized on the second edge of the horizontal pulse HSYNC inputs on Pin 24. An automatic function allows to use positive or negative horizontal pulse on Pin 24 (see Figure 2).

Figure 2



In both case BPCP width is adjustable by I^2C, B1 and B2 of register R8 (see R8 Table P8).

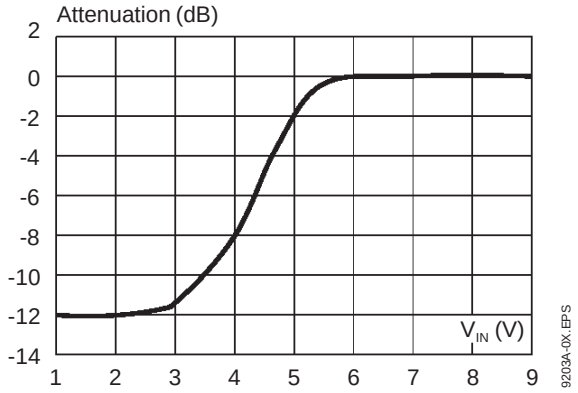
Contrast Adjustment (8 bits)

The contrast adjustment is made by controlling simultaneously the gain of three internal variable gain amplifiers through the I^2C bus interface.
The contrast adjustment allows to cover a typical range of 48dB.

ABL Control

The TDA9203A I^2C preamplifier provides an ABL input (automatic beam limitation) to attenuate R,G,B video signals according to beam intensity.
The operating range is 2.5V typicaly, from 5.3V to 2.8V. A typical 12dB Max. attenuation is applied to the signal whatever the current gain is. Refer to Figure 3 for ABL input attenuation range.
In case of software control, the ABL input must be pulled to AV_{DD} through a resistor to limit power consumption (see Figure 11).
ABL input voltage must not exceeed AV_{DD}. Input resistor is 10kΩ and equivalent schematic given in Figure 11.

Figure 3



Brightness Adjustment (8 bits)

As for the contrast adjustment, the brightness is controlled by I^2C.
The brightness function consists to add the same DC offset to the three R, G, B signals after contrast amplification. This DC-Offset is present only outside the blanking pulse (see Figure 4).
The DC output level during the blanking pulse, is forced to "INFRA-BLACK" level (V_{DC}).

Drive Adjustment (3 x 8 bits)

In order to adjust the white balance , the TDA9203A offers the possibility to adjust separately the overall gain of each complete video channel. The gain of each channel is controlled by I^2C (8bits each).
The very large drive adjustment range (48dB) allows different standard or custom color temperature.
It can also be used to adjust the output voltages at the optimum amplitude to drive the C.R.T drivers, keeping the whole contrast control for end-user only.

The drive adjustment is located after the CONTRAST, BRIGHTNESS and OSD switch blocks, so that the white balance will remains correct when BRT is adjusted, and will also be correct on OSD portion of the signal.

FUNCTIONAL DESCRIPTION (continued)

OSD Inputs

The TDA9203A includes all the circuitry necessary to mix OSD signals into the RGB main-picture. Four pins are dedicated to this function as follow.
Three TTL RGB On Screen Display inputs (Pin 2, 5 and 8). These three inputs are connected to the three outputs of the corresponding ON-SCREEN-DISPLAY processor (ex : STV942x).
One Fast Blanking Input (FBLK, Pin 13) which is also connected to the FBLK output of the same ON-SCREEN-DISPLAY processor.

When a high level is present on FBLK, the IC will acts as follow :

- The three main picture RGB input signals are internally switched to the internal input clamp reference voltage.
- The three output signals are set to voltages corresponding to the state (0 or 1) on the three OSD inputs (see Figure 4).

Example :
If FBLK = 1 and OSD1, OSD2, OSD3) = 1, 0, 1 respectively.
Then OUT1, OUT2, OUT3 will be equal to V_{OSD}, V_{BRT}, V_{OSD},
where : $V_{BRT} = V_{BLACK} + BRT$, $V_{OSD} = V_{BRT} + OSD$
BRT is the brightness DC level I^2C adjustable.
OSD is the On-Screen Display signal value I^2C adjustable from 0V to $5.5V_{PP}$ by step of 0.36V.

Semi-transparent function is controlled thanks to Bit 6 of R8 register (see Table 1).
When semi-transparent mode is activated, video signal is divided by 2 (CONT).

Table 1

FBLK	OSD1	OSD2	OSD3	B6R8	Output Signal (OUTn)
0	x	x	x	0	Video
1	x	x	x	0	OSD (1)
0	x	x	x	1	Video
1	0	x	x	1	OSD
1	x	1	x	1	OSD
1	x	x	0	1	OSD
1	1	0	1	1	Semi-transparent (2)

Notes : 1. All OSD colors are displayed.
2. One OSD color is displayed as semi-transparent video without effect on brightness and DC level adjustment.

Output Stage

The three output stages incorporate three functions which are :

- The blanking stage : When high level is applied to the BLK input (Pin 14), the three outputs are switched to a voltage which is 400mV lower than the BLACK level. The black level is the output voltage with minimum brightness when input signal video amplitude is equal to "0".
- The output stage itself : It is a large bandwidth output amplifier which allow to deliver up to $5V_{PP}$ on the three outputs (for 0.7V video signal on the inputs).
- The output CLAMP : The IC also incorporates three internal output clamp (sample and hold system) which allow to DC shift the three output signals. The DC output voltage is adjustable through I^2C with 4 bits. Practicaly, the DC output level allow to adjust the BLK level (V_{DC} = 400mV under V_{BLACK}) from 0.9V to 2.9V with 12 x 165mV.

The overall waveforms of the output signal according to the different adjustment are shown in Figures 4 and 5.

Serial Interface

The 2-wires serial interface is an I^2C interface.
The slave address of the TDA9203A is DC (in hexadecimal).

A6	A5	A4	A3	A2	A1	A0	W
1	1	0	1	1	1	0	0

Data Transfer

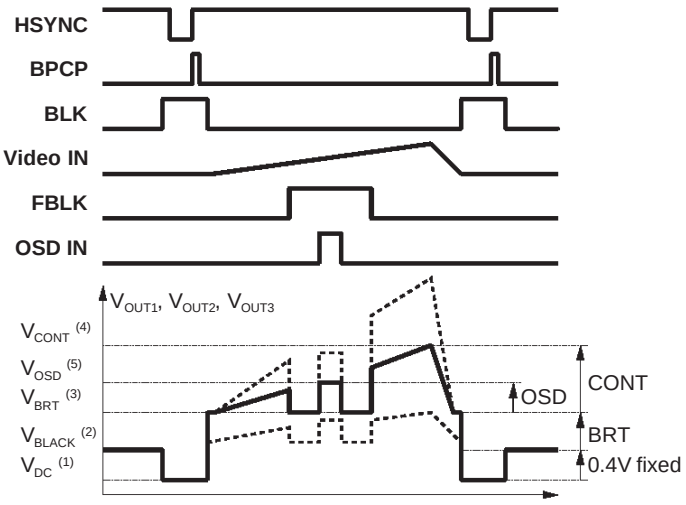
The host MCU can write data into the TDA9203A registers. Read mode is not available.
To write data into the TDA9203A, after a start, the MCU must send (see Figure 6) :

- The I^2C address slave byte with a low level for the R/W bit.
- The byte of the internal register address where the MCU wants to write data(s).
- The data.

All bytes are sent MSB bit first and the write data transter is closed by a stop.

FUNCTIONAL DESCRIPTION (continued)

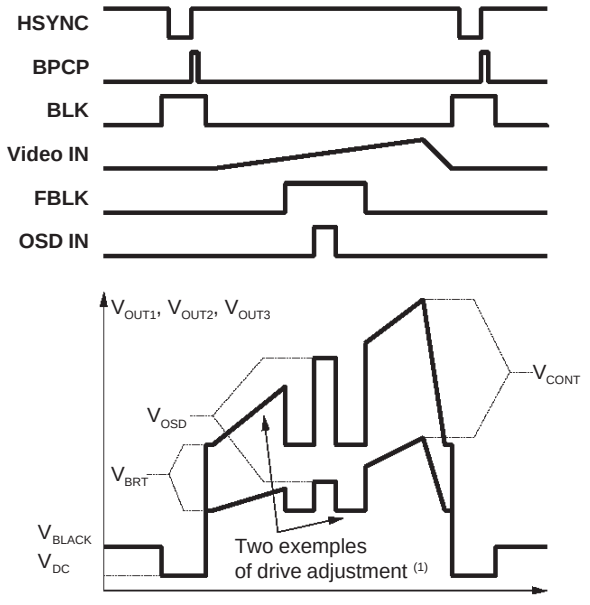
Figure 4 : Waveforms VOUT, BRT, CONT, OSD



Notes :
1. V_{DC} = 0.5 to 2.5V
2. $V_{BLACK} = V_{DC}$ + 0.4V
3. $V_{BRT} = V_{BLACK}$ + BRT (with BRT = 0 to 2.5V)
4. $V_{CONT} = V_{BRT}$ + CONT with CONT = k x Video IN (CONT = $5V_{PP}$ max. for $V_{IN} = 0.7V_{PP}$)
5. $V_{OSD} = V_{BRT}$ + OSD with OSD = k1 x OSDIN (OSD max. = $5.5V_{PP}$, OSD min. = $360mV_{PP}$)

9203A-06.EPS

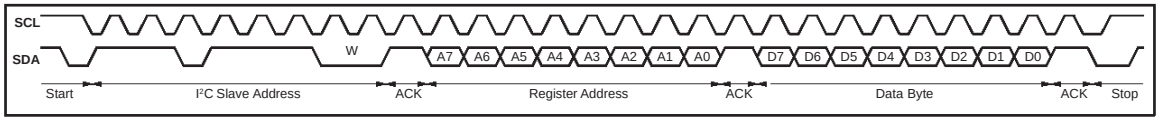
Figure 5 : Waveforms (DRIVE adjustment)



Note : 1. Drive adjustment modifies the following voltages : V_{CONT}, V_{BRT} and V_{OSD}.
Drive adjustment do not modify the following voltages : V_{DC} and V_{BLACK}.

9203A-07.EPS

Figure 6 : I^2C Write Operation



9203A-08.EPS

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Signal Bandwidth ($4V_{PP}$/12pF load)		70		MHz
	Rise and Fall Time ($4V_{PP}$/12pF load)		5.5		ns
	Drive Adjustment Range on the 3 Channels separately		48		dB
	Maximum Output Voltage (V_{IN} = 0.7 V_{PP})		5		V_{PP}
	Output Voltage Range (AC + DC)			8	V

9203A-02.TBL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (Pins 3-9-17-20-23)	14	V
V_{IN1}	Voltage at any Input Pins (except SDA & SCL & Logical Inputs)	GND < V_{IN1} < V_S	V
V_{IN2}	Voltage at Input Pins SDA & SCL	GND < V_{IN2} < 5.5	V
V_{IN3}	Voltage at Logical Inputs (OSD, FBLK, BLK, HSYNC)	GND < V_{IN3} < 5.5	V
V_{ESD}	ESD Susceptability (Human body model ; 100pF Discharge through 1.5kΩ)	2	kV
T_{stg}	Storage Temperature	- 40, + 150	°C
T_j	Junction Temperature	150	°C
T_{oper}	Operating Temperature	0, + 70	°C

9203A-03.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	69	°C/W

9203A-04.TBL

DC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC} = 12V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	Pins 3-9-17-20-23	10.8	12	13.2	V
I_S	Supply Current (All V_S Pin current)	R_L = 1kΩ		60		mA
V_I	Video Input Voltage Amplitude	Pins 1-4-7		0.7	1	V_{PP}
V_O	Typical Output Voltage Range	Pins 16-19-22	0.5	-	8	V
V_{IL}	Low Level Input (OSD, FBLK, BLK, HSYNC)	Pins 2-5-8-13-14-24			0.8	V
V_{IH}	High Level Input (OSD, FBLK, BLK, HSYNC)	Pins 2-5-8-13-14-24	2.4			V
I_{IN}	Input Current (OSD, FBLK, BLK, HSYNC)	0.4V < V_{IN} < 4.5V	-10		+10	µA

9203A-05.TBL

AC ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, V_{CC} = 12V, C_L = 12pF, R_L = 1kΩ , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AV	Maximum Gain (20 log x $V_{OUT\ AC}/V_{IN\ AC}$)	Contrast & Drive at maximum		18		dB
CAR	Contrast Attenuation Range	V_{IN} = 0.7V_{PP}, Contrast & Drive at POR		48		dB
DAR	Drive Attenuation Range			48		dB
GM	Gain Match	V_{OUT} = 2.5V_{PP}, V_{IN} = 0.7V_{PP} Contrast = Drive = Maxi x 0.7 (power-on reset value)		± 0.1		dB
BW	Bandwidth Large Signal	At -3dB, V_{IN} = 0.7V_{PP}, V_{OUT} = 4V_{PP} Contrast = Drive = Maxi x 0.87		70		MHz
DIS	Video Output Distorsion (see Note)	f = 1MHz, V_{OUT} = 1V_{PP}, V_{IN} = 1V_{PP}		0.3		%
t_R, t_F	Video Output Rise and Fall Time (see Note)	VIN = 0.7V_{PP}, V_{OUT} = 4V_{PP} Contrast = Drive = Maxi x 0.87		5.5		ns
BRT	Brightness Maximum DC Level Brightness Minimum DC Level			2.5 0		V V
BRTM	Brightness Matching	BRT = 50%, Drive at POR		±20		mV
OSD CAR	Contrast Attenuation Range for OSD Input			24		dB
DC	Output Maximum DC Level Output Minimum DC Level			2.5 0.5		V V
R_L	Equivalent Load on Video Output	with $T_j \leq T_{j\ Max.}$		1		kΩ
CT	Croostalk between Video Channels (see Note)	V_{OUT} = 2.5V_{PP}, V_{IN} = 0.7V_{PP} Contrast = Drive = Maxi x 0.7 (power-on reset value) f_{IN} = 1MHz	44			dB
G_{ABL}	ABL Min. Attenuation ABL Max. Attenuation	V_{ABL} = 5.3V Typical V_{ABL} = 2.8V Typical		0 12		dB dB
I_{ABL}	ABL Input Current	V_{ABL} = 5.3V		20		µA
R_{ABL}	ABL Input Resistor	See Figure 11		10		kΩ

9203A-06.TBL

Note : These parameters are not tested on each unit. They are measured during an internal qualification procedure which includes characterization on batches coming from corners of our processes and also from temperature characterization.

I^2C ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC} = 12V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage	On Pins SDA, SCL			1.5	V
V_{IH}	High Level Input Voltage		3			V
I_{IN}	Input Current (Pins SDA, SCL)	0.4V < V_{IN} < 4.5V	-10		+10	µA
$f_{SCL(Max.)}$	SCL Maximum Clock Frequency		200			kHz
V_{OL}	Low Level Output Voltage	SDA Pin when ACK Sink Current = 6mA			0.6	V

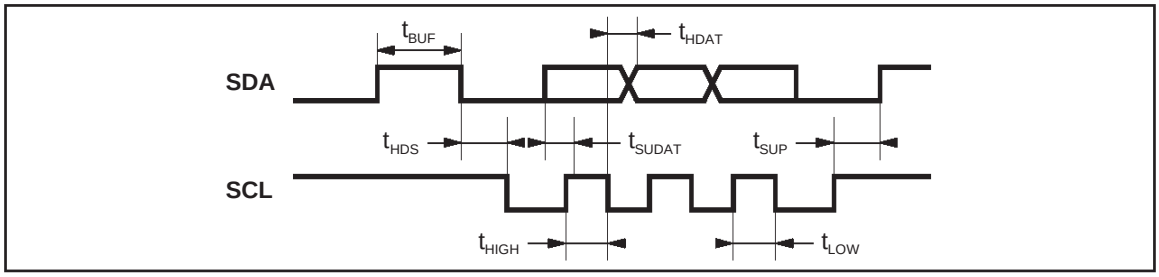
9203A-08.TBL

I^2C INTERFACE TIMINGS REQUIREMENTS (see Figure 7)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{BUF}	Time the bus must be free between 2 access	1300			ns
t_{HDS}	Hold Time for Start Condition	600			ns
t_{SUP}	Set-up Time for Stop Condition	600			ns
t_{LOW}	The Low Period of Clock	1300			ns
t_{HIGH}	The High Period of Clock	600			ns
t_{HDAT}	Hold Time Data	300			ns
t_{SUDAT}	Set-up Time Data	250			ns
t_R, t_F	Rise and Fall Time of both SDA and SCL	20		300	ns

9203A-09.TBL

Figure 7



9203A-09.EPS

REGISTER DESCRIPTION

Registers Sub-address

Address (Hex)	Register Names	Function	POR Value
01	Contrast	DAC 8-bit	B4
02	Brightness	DAC 8-bit	B4
03	Drive 1	DAC 8-bit	B4
04	Drive 2	DAC 8-bit	B4
05	Drive 3	DAC 8-bit	B4
06	Output DC Level	DAC 4-bit	08
07	OSD Contrast	DAC 4-bit	08
08	BP and Miscellaneous	See R8 Table	04

Contrast Register (R1) (Video IN = 0.5V_{PP}, Brightness at minimum,Drive at maximum)

Hex	b7	b6	b5	b4	b3	b2	b1	b0	CONT (V_{PP})	G (dB)	POR Value
00	0	0	0	0	0	0	0	0	0	-	
01	0	0	0	0	0	0	0	1	0.015	-30	
02	0	0	0	0	0	0	1	0	0.031	-24	
04	0	0	0	0	0	1	0	0	0.062	-18	
08	0	0	0	0	1	0	0	0	0.125	-12	
10	0	0	0	1	0	0	0	0	0.25	-6	
20	0	0	1	0	0	0	0	0	0.5	0	
40	0	1	0	0	0	0	0	0	1	6	
80	1	0	0	0	0	0	0	0	2	12	
B4	1	0	1	1	0	1	0	0	2.812	15	X
FF	1	1	1	1	1	1	1	1	4	18	

Brightness Register (R2) (Drive at maximum)

Hex	b7	b6	b5	b4	b3	b2	b1	b0	BRT (V)	POR Value
00	0	0	0	0	0	0	0	0	0	
01	0	0	0	0	0	0	0	1	0.010	
02	0	0	0	0	0	0	1	0	0.020	
04	0	0	0	0	0	1	0	0	0.040	
08	0	0	0	0	1	0	0	0	0.080	
10	0	0	0	1	0	0	0	0	0.160	
20	0	0	1	0	0	0	0	0	0.320	
40	0	1	0	0	0	0	0	0	0.640	
80	1	0	0	0	0	0	0	0	1.28	
B4	1	0	1	1	0	1	0	0	1.8	X
FF	1	1	1	1	1	1	1	1	2.56	

REGISTER DESCRIPTION (continued)

Drive Registers (R3, R4, R5) (Video IN = 0.5V_{PP}, Brightness at minimum, Contrast at maximum)

Hex	b7	b6	b5	b4	b3	b2	b1	b0	CONT (V_{PP})	G (dB)	POR Value
00	0	0	0	0	0	0	0	0	0	-	
01	0	0	0	0	0	0	0	1	0.015	-30	
02	0	0	0	0	0	0	1	0	0.031	-24	
04	0	0	0	0	0	1	0	0	0.062	-18	
08	0	0	0	0	1	0	0	0	0.125	-12	
10	0	0	0	1	0	0	0	0	0.25	-6	
20	0	0	1	0	0	0	0	0	0.5	0	
40	0	1	0	0	0	0	0	0	1	6	
80	1	0	0	0	0	0	0	0	2	12	
B4	1	0	1	1	0	1	0	0	2.812	15	X
FF	1	1	1	1	1	1	1	1	4	18	

Output DC Level Register (R6)

Hex	b7	b6	b5	b4	b3	b2	b1	b0	DC (V)	POR Value
03	0	0	0	0	0	0	1	1	0.52	
04	0	0	0	0	0	1	0	0	0.69	
08	0	0	0	0	1	0	0	0	1.35	X
0F	0	0	0	0	1	1	1	1	2.5	

Code 00Hex, 01Hex and 02Hex : not to be used

OSD Contrast Register (R7) ($V_{OSD\ IN}$ = 2.4V_{Min}.., Drive at maximum)

Hex	b7	b6	b5	b4	b3	b2	b1	b0	OSD (V)	G (dB)	POR Value
00	0	0	0	0	0	0	0	0	0	-	
01	0	0	0	0	0	0	0	1	0.36	-24	
02	0	0	0	0	0	0	1	0	0.73	-18	
04	0	0	0	0	0	1	0	0	1.46	-12	
08	0	0	0	0	1	0	0	0	2.93	-6	X
0F	0	0	0	0	1	1	1	1	5.5	0	

BP and Miscellaneous Register (R8)

b7	b6	b5	b4	b3	b2	b1	b0	Function	POR Value
							0	BP Source = HSYNC	X
							1	BP Source = BLK	
					0	0		BP Pulse Width = 0.33µs	
					0	1		BP Pulse Width = 0.66µs	
					1	0		BP Pulse Width = 1µs	X
					1	1		BP Pulse Width = 1.3µs	
			0	0				Test Purposes	X
		0	0	0				Soft Blanking OFF	X
		1	1	1				Soft Blanking ON	
	0							Semi Transparent OFF	X
	1							Semi Transparent ON	
0								Positive Blanking Polarity Selection	X
1								Negative Blanking Polarity Selection	

INTERNAL SCHEMATICS

Figure 8

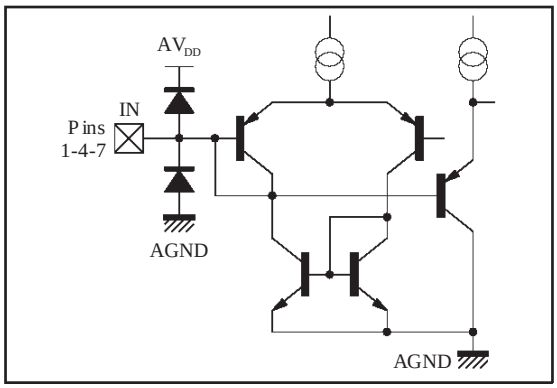


Figure 9

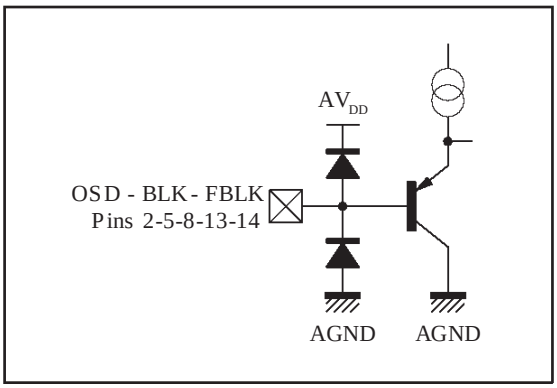


Figure 10

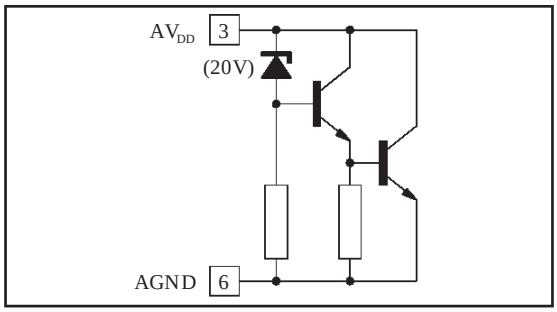


Figure 11

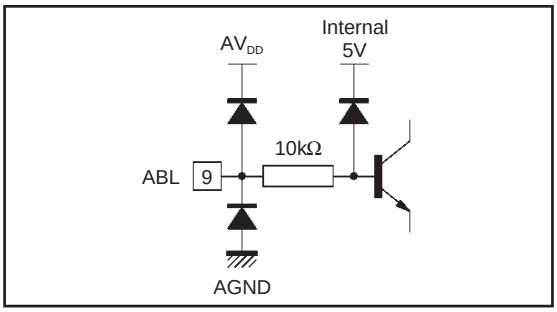


Figure 12

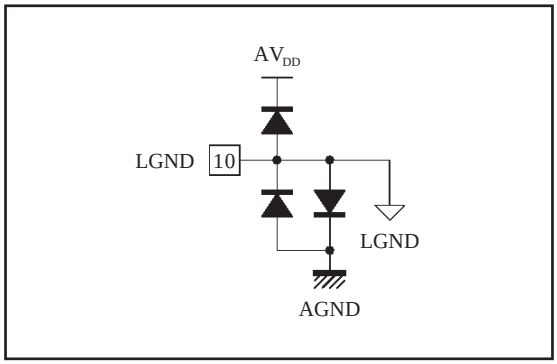


Figure 13

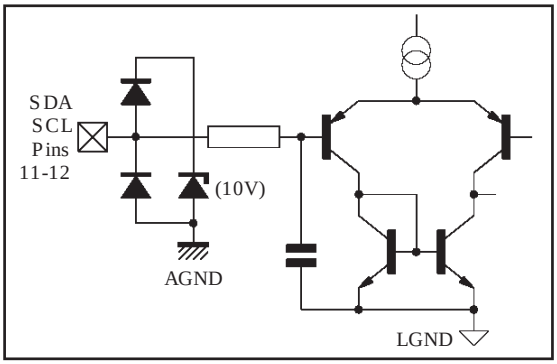


Figure 14

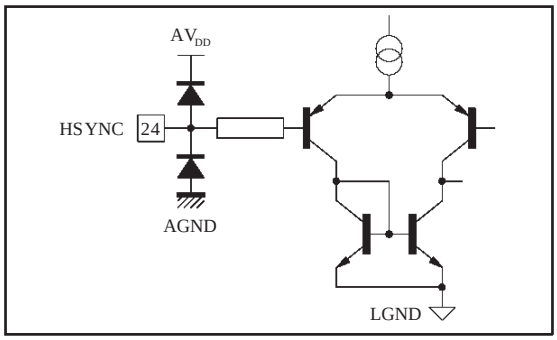
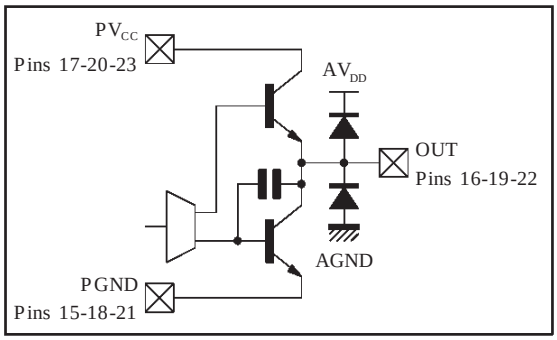
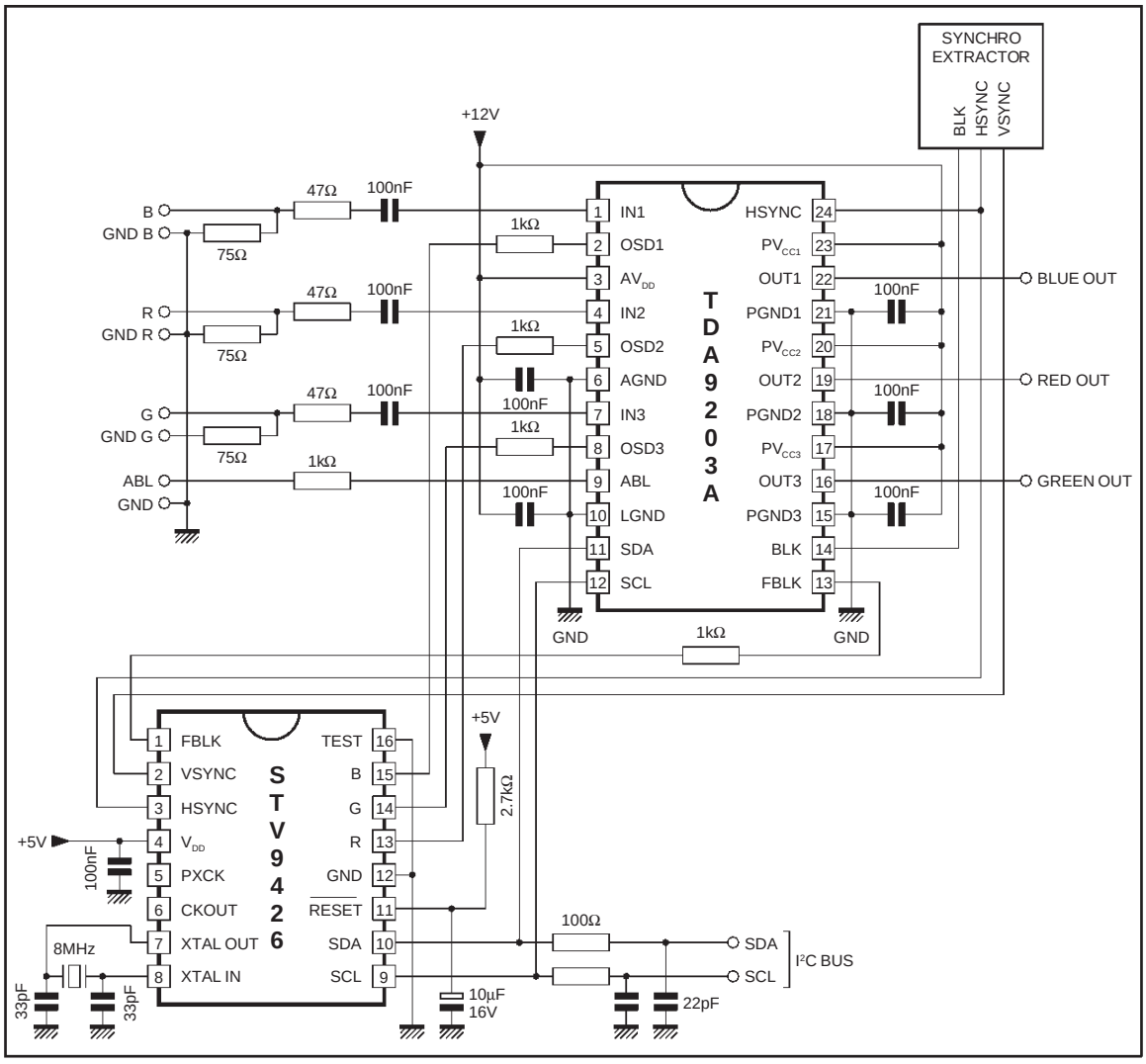


Figure 15

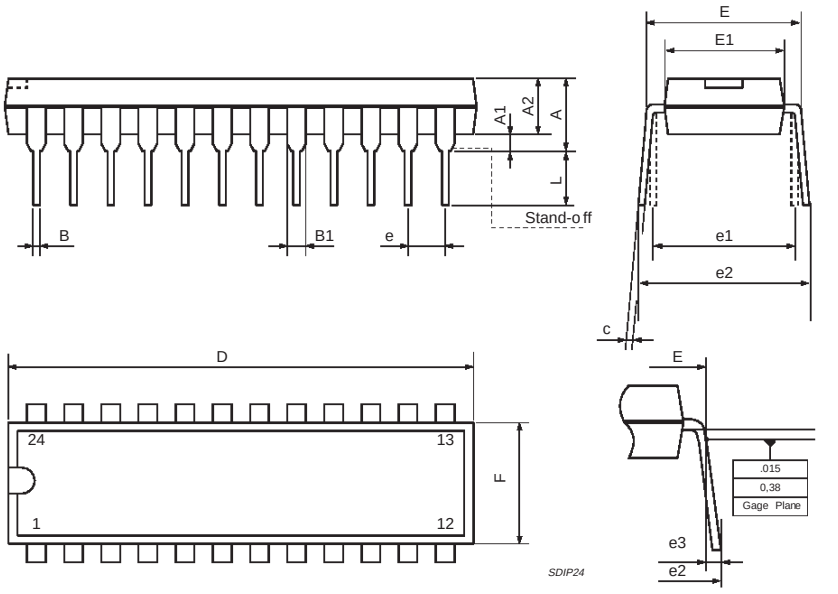


APPLICATION DIAGRAM



PACKAGE MECHANICAL DATA

24 PINS - PLASTIC DIP (SHRINK)



PMSDIP24.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.20
A1	0.51			0.020		
	3.05	3.30	4.57	0.120	0.130	0.180
B	0.36	0.46	0.56	0.0142	0.0181	0.0220
B1	0.76	1.02	1.14	0.030	0.040	0.045
C	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	22.61	22.86	23.11	0.890	0.90	0.910
E	7.62		8.64	0.30		0.340
E1	6.10	6.40	6.86	0.240	0.252	0270
e		1.778			0.070	
e1		7.62			0.30	
e2			10.92			0.430
e3			1.52			0.060
L	2.54	3.30	3.81	0.10	0.130	0.150

SDIP24.TBL