

## RGB MATRIX PREAMPLIFIER

The TDA2530 is an integrated RGB matrix preamplifier for colour television receivers, incorporating a matrix preamplifier for RGB cathode drive of the picture tube with clamping circuits. The three channels have the same layout to ensure identical frequency behaviour.

This integrated circuit has been designed to be driven from the TDA2522 synchronous demodulator and oscillator IC.

### QUICK REFERENCE DATA

Supply voltage	$V_{9-16}$	typ.	12 V
Operating ambient temperature range	$T_{amb}$		-20 to +60 °C
Luminance input resistance	$R_{1-16}$	>	100 k $\Omega$
Input current of colour difference inputs	$I_2, I_4, I_6$	typ.	2 $\mu$ A
during clamping	$I_2, I_4, I_6$		-0, 2 to +0, 2 mA
Clamping pulse input current	$-I_8$	<	20 $\mu$ A
Gain of RGB preamplifiers	G	typ.	0 dB
Gain d. c. adjustment range	$\Delta G$	typ.	$\pm 3$ dB
Gain of error amplifier (conductance)		typ.	20 mA/V
Input current of feedback inputs	$I_{11}, I_{13}, I_{15}$	typ.	2 $\mu$ A
Output current swing	$I_{10}, I_{12}, I_{14}$		-4, 4 to +4, 4 mA

### PACKAGE OUTLINES

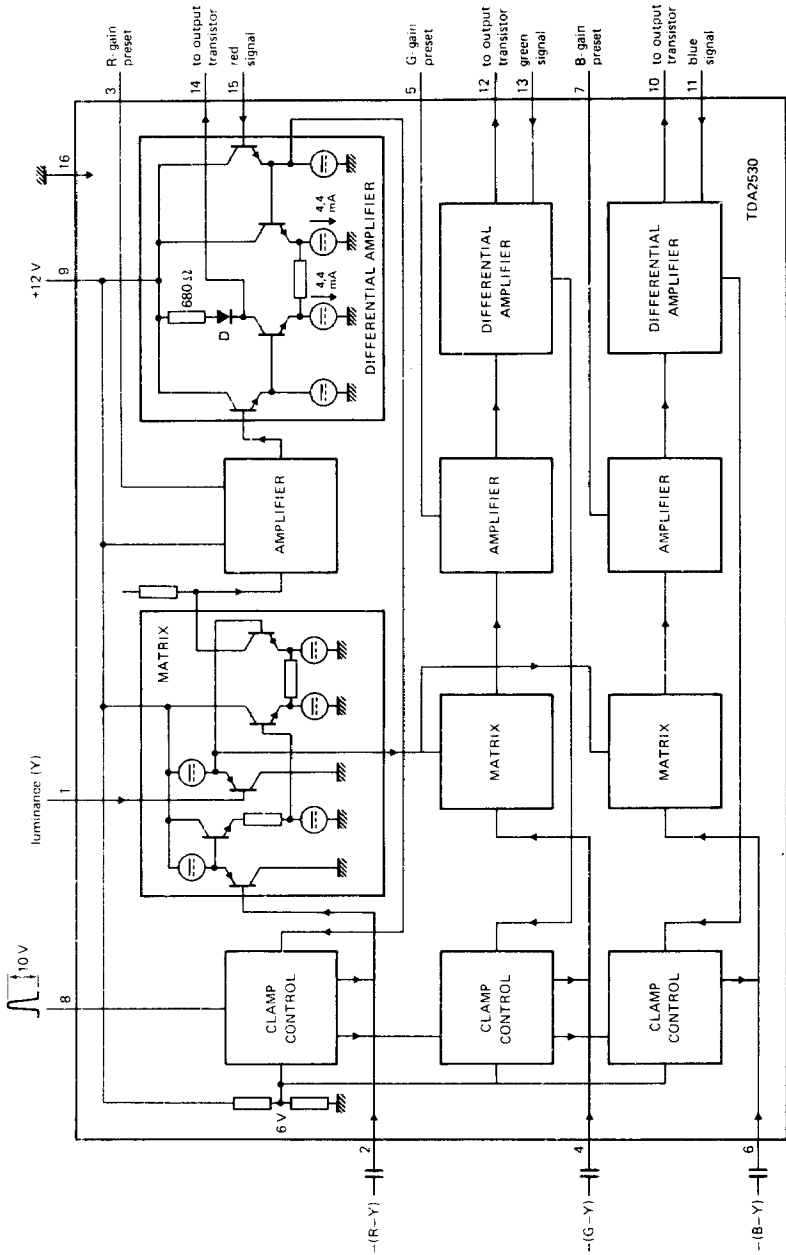
TDA2530 : 16-lead DIL; plastic (SOT-38).

TDA2530Q : 16-lead QIL; plastic (SOT-58).

TDA2530  
TDA2530Q



BLOCK DIAGRAM



7275189

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Supply voltage (pin 9)	$V_P$ (V <sub>9-16</sub> ) max.	15 V
Pin 1	$V_{1-16}$	0 to $V_P$
Pins 3, 5 and 7	$V_{3;5;7-16}$	0 to $V_P$
Pins 2, 4 and 6	$V_{2;4;6-16}$	0 to $V_P$
Pin 8	$V_{8-16}$ max.	$V_P$
Pin 10	$V_{10-16}$	$V_{11-16}$ to $V_P + 3$ V
Pin 12	$V_{12-16}$	$V_{13-16}$ to $V_P + 3$ V
Pin 14	$V_{14-16}$	$V_{15-16}$ to $V_P + 3$ V
Pins 11, 13 and 15	$V_{11;13;15-16}$	0,3 $V_P$ to $V_P$

Current

Pin 8	$-I_8$	max.	1 mA
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Power dissipation

Total power dissipation	$P_{tot}$	max.	1 W
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Temperatures

Storage temperature	$T_{stg}$	-20 to +125 °C
Operating ambient temperature	$T_{amb}$	-20 to +60 °C

**CHARACTERISTICS** at  $V_P = 12$  V;  $V_{1-16} = 1,5$  V;  $T_{amb} = 25$  °C; measured in circuit on page 5.

Current consumption	$I_9$	typ.	50 mA
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**Luminance input**

Black level	$V_{1-16}$	typ.	1,5 V
Black-to-white input voltage (peak-to-peak value)	$V_{1-16(p-p)}$	typ.	1,0 V
Input resistance	$R_{1-16}$	>	100 k $\Omega$

**Colour difference input**

Input signals (peak-to-peak values)	R-Y 1)	$V_{2-16(p-p)}$	typ.	1,4 V
	G-Y 1)	$V_{4-16(p-p)}$	typ.	0,82 V
	B-Y 1)	$V_{6-16(p-p)}$	typ.	1,78 V

Input currents (source resistance 300 $\Omega$ max.)	$I_2, I_4, I_6$	typ.	2 $\mu$ A
		<	4 $\mu$ A

Input currents during clamping	$I_2, I_4, I_6$	-0,2 to +0,2 mA
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1) This prescribed order is not mandatory, as all three channels are identical.

**CHARACTERISTICS** (continued)

**Clamp pulse input for d.c. feedback**

Input voltage for clamping: on level	$V_{8-16}$		6, 5 to 12	V
off level	$V_{8-16}$		0 to 5, 5	V <sup>1)</sup>
Input current for clamping: on level	$I_8$	<	1	$\mu\text{A}$
off level	$-I_8$	<	20	$\mu\text{A}$

**Feedback input**

D.C. level during clamping	$V_{11;13;15-16}$	typ.	0, 5	V <sub>P</sub>
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**Gain adjustment for colour drive**

Adjustment voltage range	$V_{3;5;7-16}$		0 to 10	V
Adjustment voltage for nominal gain	$V_{3;5;7-16}$	typ.	5	V
Nominal gain between colour difference inputs, luminance input and colour feedback inputs (pins 11, 13 and 15)	G	typ.	0	dB <sup>2)</sup>
Adjustment range of nominal gain at $\Delta V_{3;5;7-16} = \pm 5$ V	$\Delta G$	>	$\pm 3$	dB

**Differential amplifier**

Input current of feedback inputs	$I_{11}, I_{13}, I_{15}$	typ.	2	$\mu\text{A}$
Gain of error amplifier (conductance)		typ.	20	mA/V
Output current swing	$I_{10}, I_{12}, I_{14}$		-4, 4 to +4, 4	mA
Integrated load resistance	$R_{10;12;14-9}$	typ.	680	$\Omega$ <sup>3)</sup>
Output bias voltage (see application information)	$V_{10;12;14-16}$	typ.	8	V <sup>3)</sup>

**APPLICATION INFORMATION** (see circuit on page 5)

Clamping level ( $V_{cl}$ ) of video output stages, with set clamping level potentiometers in their mid-positions:

$$V_{cl} = V_P \left( 1 + \frac{R_1}{R_2} - \frac{R_1}{R_3} \right)$$

$$\text{Gain of video output stages: } G = 1 + \frac{R_1}{R_2} + \frac{R_1}{R_3} + \frac{R_1}{R_4}$$

1) Switching from clamping on to off occurs at about 6 V.

2) Error signal is assumed to be negligible.

3) The fact that the load resistors have series diodes (D; see block diagram on page 2), means that the resistors can be ignored when  $V_{10;12;14} \geq V_P$ . In that case, external load resistors must be chosen such that the nominal current will be 4, 4 mA.

APPLICATION INFORMATION

