Ordering number : EN2624E

SANYO Semiconductors
DATA SHEET

LA6510 — Monolithic Linear IC
Dual Power Operational Amplifier

Overview

The LA6510 is a dual power operational amplifier IC capable of delivering larger output currents than conventional operational amplifiers.
The LA6510 features an on-chip current limiter and provides high voltage gain and a high common-mode rejection ratio.
The LA6510 is an ideal choice for power applications such as DC servos, capstan drivers, actuator drivers, programmable power supplies and high-quality audio amplifiers.

Functions

- High output current (I_O max = 1.0A)
- High gain
- Equipped with current limiter pin
- Supports single power source operation

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} / V_{EE} max		±18	V
Differential input voltage	V_{ID}		30	V
Common mode input voltage	V_{ICOM}		±15	V
Maximum output current	I_O max		1.0	A
Allowable power dissipation	Pd max		2.5	W
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

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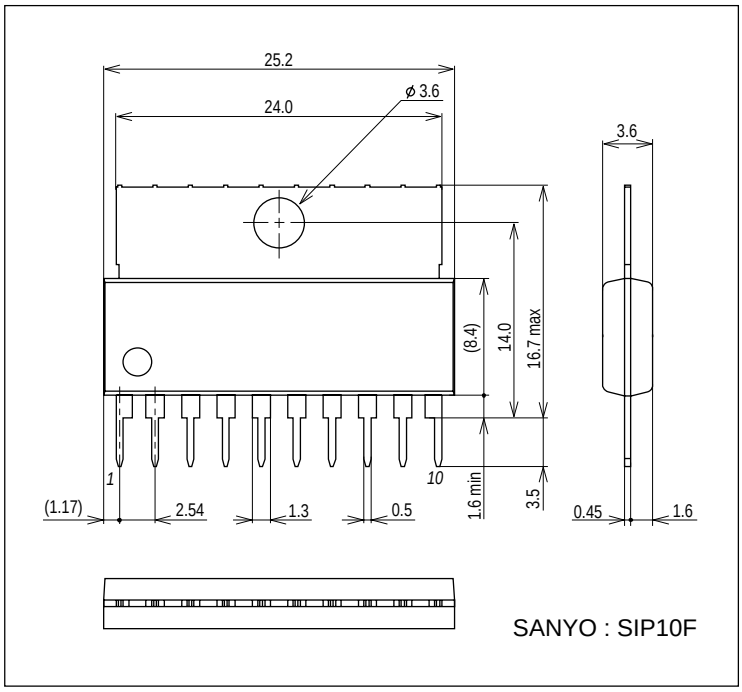
Electrical Characteristics at Ta = 25°C, V_{CC} / V_{EE} = ±15V

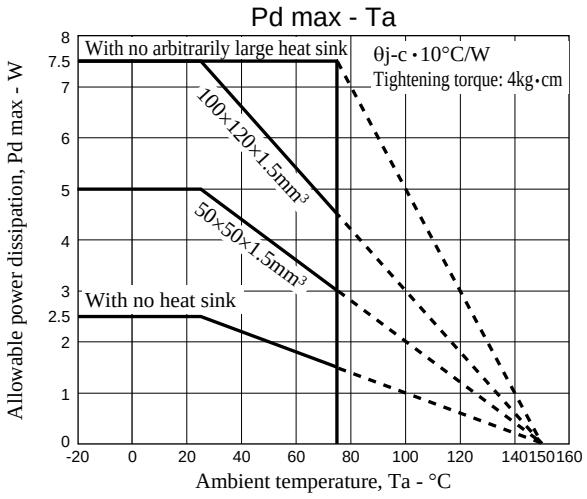
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
No-load current drain	I_{CCO}			12	20	mA
Input offset voltage	V_{IO}	$R_S \leq 10k\Omega$		2	6	mV
Input offset current	I_{IO}			10	200	nA
Input bias current	I_B			100	700	nA
Common-mode input voltage range	V_{ICM}		-15		+13	V
Common-mode signal rejection ratio	C_{MR}		70	80		dB
Output voltage	V_O	R_L=33Ω	±12	±13		V
Voltage gain	VG_O			100		dB
Slew rate	SR	G_V = 0, R_L= 33Ω, R = 2.2Ω, C = 0.1μF		0.15		V/μs
Equivalent input noise voltage	V_{NI}	Rg = 1kΩ, DIN AUDIO		2		μV
Supply voltage rejection ratio	SVR			30	150	μV/V
Limiting current	I_{SC}	Rsc = 2.2Ω		0.35		A

Package Dimensions

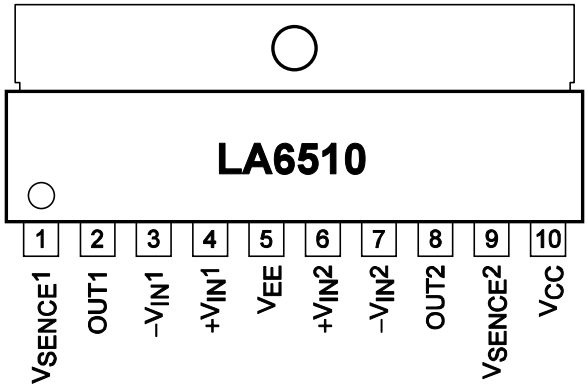
unit : mm (typ)

3046D

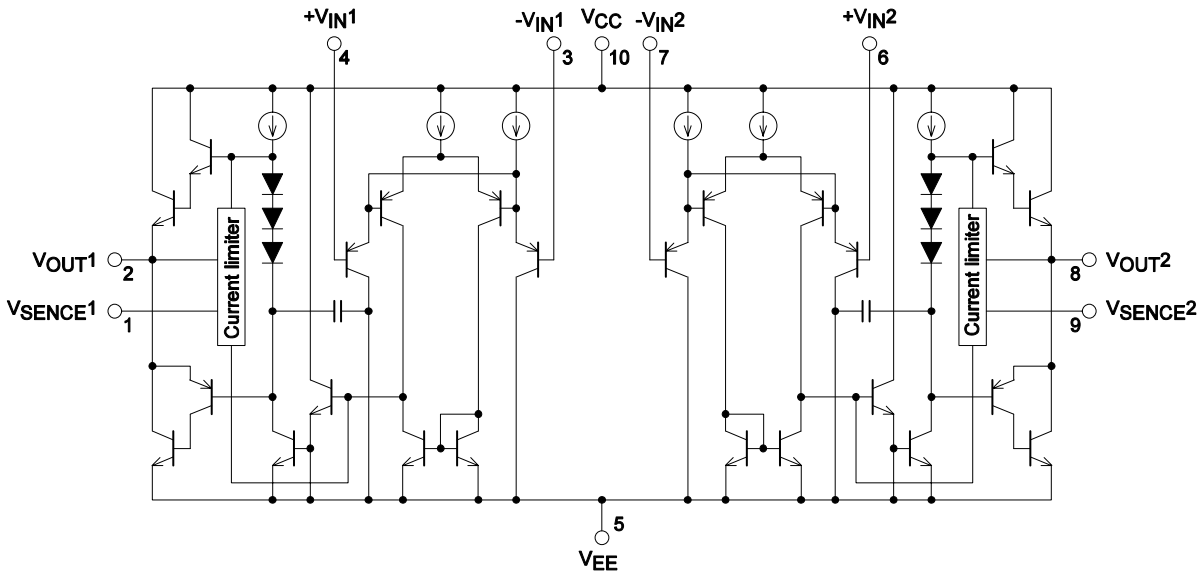




Pin Assignment

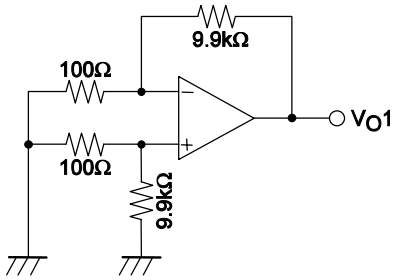


Equivalent Circuit



Test Circuits

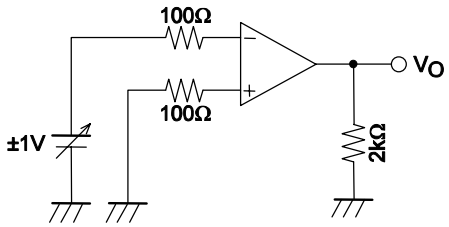
1. Input offset voltage [V_{IO}]
   Supply voltage rejection ratio [SVR]



V_{IO} V_{CC} / V_{EE} = ±15V

SVR $\begin{bmatrix} V_{CC} = 15V,5V \\ V_{EE} = -5V,-15V \end{bmatrix}$

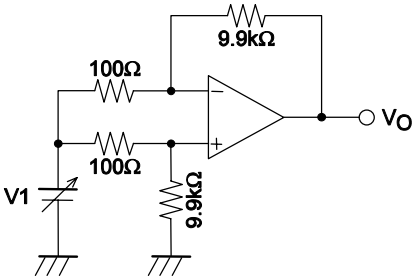
2. Output voltage [V_O]



$V_{IO} = V_O1 / 100$

$$\begin{matrix} SVR(+) \\ SVR(-) \end{matrix} \Big] = \left| \frac{\Delta V_O1}{100 \times 10V} \right|$$

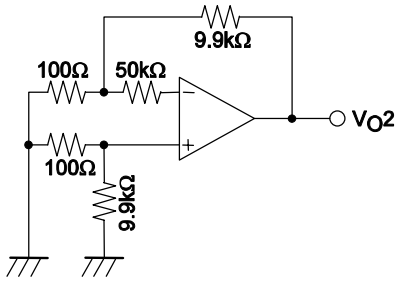
3. Common-mode signal rejection ratio [CMR]
   Common-mode input voltage range [V_{ICM}]



CMR V1 = ±7.5V

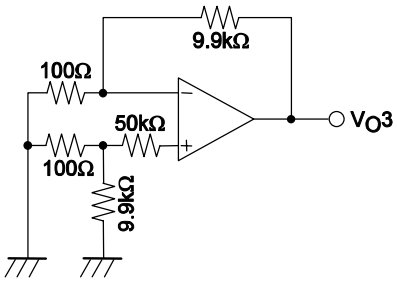
$$CMR = 20 \log \frac{15 \times 100}{|\Delta V_O'|}$$

4. Input bias current [$I_B(+)$]



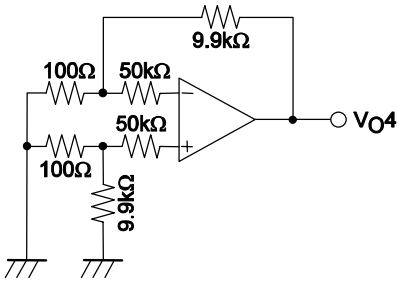
$$I_B(+) = \left| \frac{V_O2 - V_O1}{50k\Omega \times 100} \right|$$

5. Input bias current [$I_{B(-)}$]



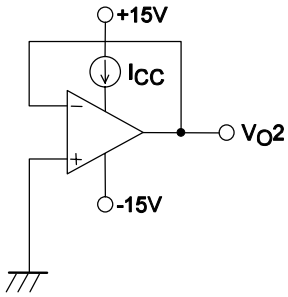
$$I_{B(-)} = \left| \frac{V_{O}3 - V_{O}1}{50k\Omega \times 100} \right|$$

6. Input offset current [I_{IO}]

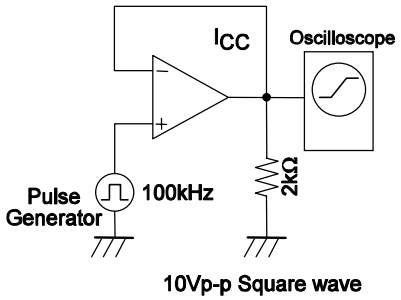


$$I_{IO} = \left| \frac{V_{O}4 - V_{O}1}{50k\Omega \times 100} \right|$$

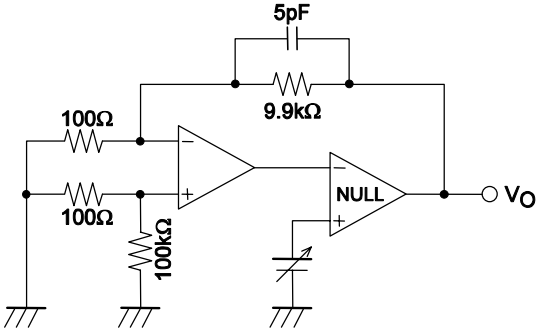
7. Current drain [I_{CC}]



8. Slew rate [SR]

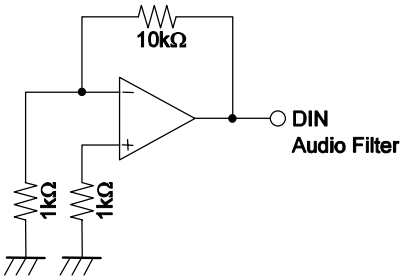


9. Voltage gain [VG_O]

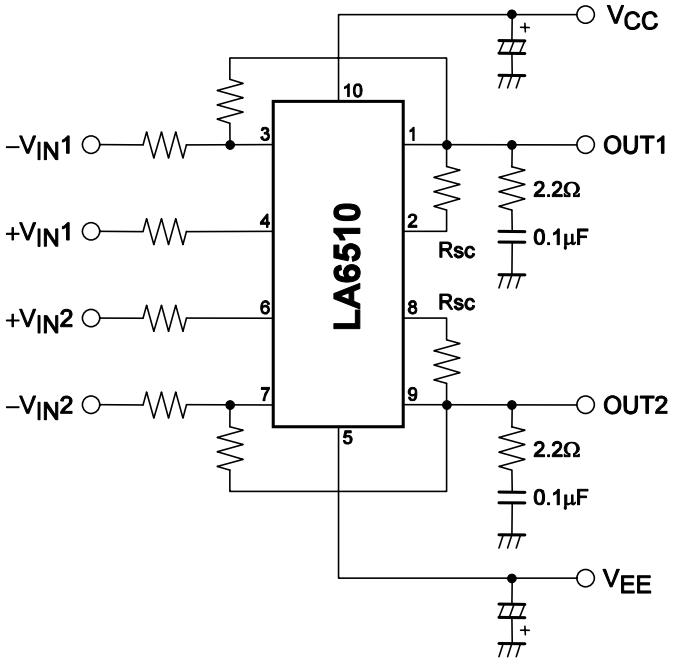


$$VG_O = 20 \log \frac{1000 \times 20}{\Delta V_O}$$

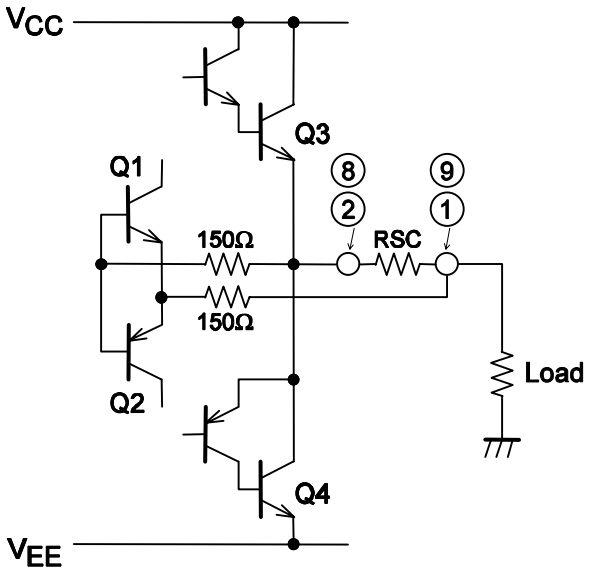
10. Equivalent input noise voltage [V_{NI}]



Application Circuit Examples



Current Limiter Circuit and Output Stage



In source mode, when Q3 turns on and current flows into the load resistor, a voltage difference occurs across RSC, turning on Q1 and activating the current limiter.

In sink mode, Q4 turns on to develop a voltage difference of the polarity opposite to that in the source mode across RSC, thus turning on Q2 and activating the limiter.
A RSC can be use to set the maximum output current, but the maximum output current will vary slightly depending on the V_{BE} temperature characteristics of the transistor.