

DATA SHEET

TDA1563Q

**2 × 25 W high efficiency car radio
power amplifier**

Product specification
Supersedes data of 1998 Jul 14
File under Integrated Circuits, IC01

2000 Feb 09

2 × 25 W high efficiency car radio power amplifier

TDA1563Q

FEATURES

- Low dissipation due to switching from Single-Ended (SE) to Bridge-Tied Load (BTL) mode
- Differential inputs with high Common Mode Rejection Ratio (CMRR)
- Mute/standby/operating (mode select pin)
- Zero crossing mute circuit
- Load dump protection circuit
- Short-circuit safe to ground, to supply voltage and across load
- Loudspeaker protection circuit
- Device switches to SE operation at excessive junction temperatures
- Thermal protection at high junction temperature (170°C)
- Diagnostic information (clip detection and protection/temperature)
- Clipping information can be selected between THD = 2.5% or 10%

GENERAL DESCRIPTION

The TDA1563Q is a monolithic power amplifier in a 17-lead DIL-bent-SIL plastic power package. It contains two identical 25 W amplifiers. The dissipation is minimized by switching from SE to BTL mode when a higher output voltage swing is needed. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _P	supply voltage	DC biased	6	14.4	18	V
		non-operating	–	–	30	V
		load dump	–	–	45	V
I _{ORM}	repetitive peak output current		–	–	4	A
I _{q(tot)}	total quiescent current	R _L = ∞	–	95	150	mA
I _{stb}	standby current		–	1	50	μA
Z _i	input impedance		90	120	150	kΩ
P _o	output power	R _L = 4 Ω; EIAJ	–	38	–	W
		R _L = 4 Ω; THD = 10%	23	25	–	W
		R _L = 4 Ω; THD = 2.5%	18	20	–	W
V _{selclip}						
G _v	closed loop voltage gain		25	26	27	dB
CMRR	common mode rejection ratio	f = 1 kHz; R _s = 0 Ω	–	80	–	dB
SVRR	supply voltage ripple rejection	f = 1 kHz; R _s = 0 Ω	45	65	–	dB
ΔV _O	DC output offset voltage		–	–	100	mV
α _{cs}	channel separation	R _s = 0 Ω	40	70	–	dB
ΔG _v	channel unbalance		–	–	1	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1563Q	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

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BLOCK DIAGRAM

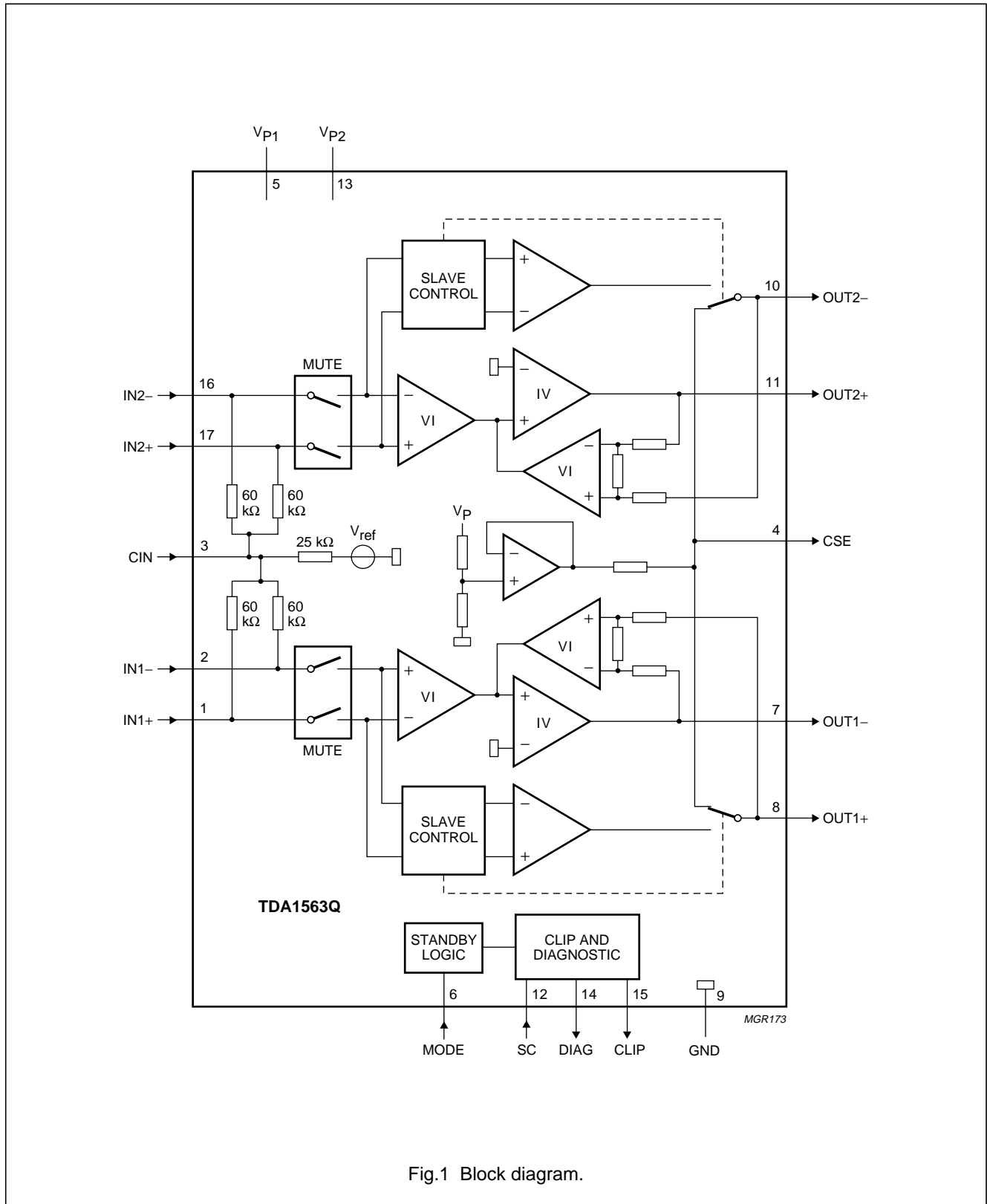


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
IN1+	1	non-inverting input 1
IN1-	2	inverting input 1
CIN	3	common input
CSE	4	electrolytic capacitor for SE mode
V _{P1}	5	supply voltage 1
MODE	6	mute/standby/operating
OUT1-	7	inverting output 1
OUT1+	8	non-inverting output 1
GND	9	ground
OUT2-	10	inverting output 2
OUT2+	11	non-inverting output 2
SC	12	selectable clip
V _{P2}	13	supply voltage 2
DIAG	14	diagnostic: protection/temperature
CLIP	15	diagnostic: clip detection
IN2-	16	inverting input 2
IN2+	17	non-inverting input 2

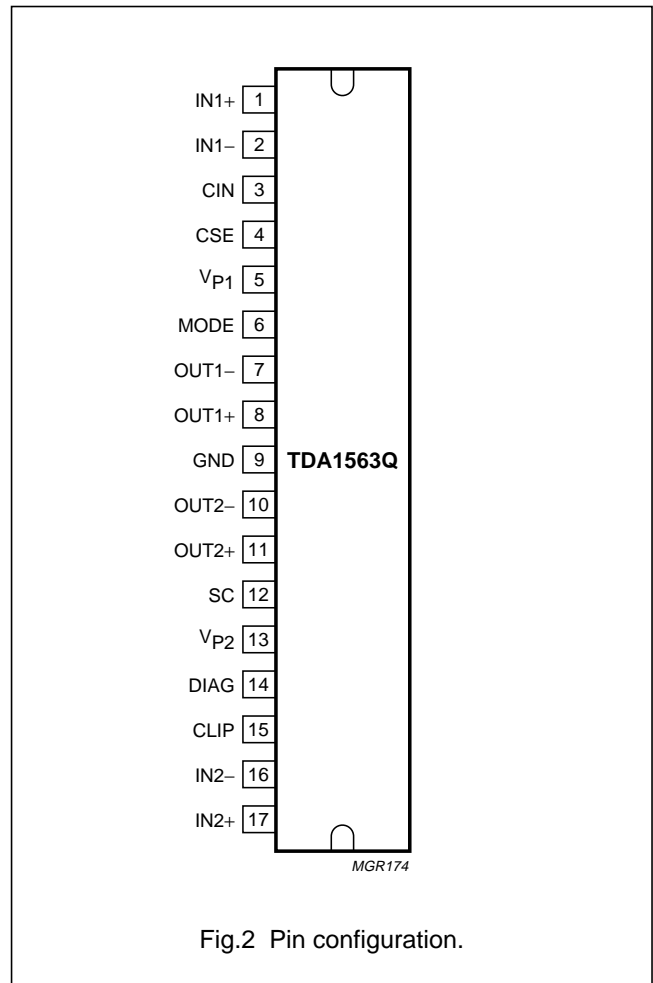


Fig.2 Pin configuration.

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FUNCTIONAL DESCRIPTION

The TDA1563Q contains two identical amplifiers with differential inputs. At low output power (up to output amplitudes of 3 V (RMS) at $V_P = 14.4$ V), the device operates as a normal SE amplifier. When a larger output voltage swing is needed, the circuit switches to BTL operation.

With a sine wave input signal, the dissipation of a conventional BTL amplifier up to 2 W output power is more than twice the dissipation of the TDA1563Q (see Fig.10).

In normal use, when the amplifier is driven with music-like signals, the high (BTL) output power is only needed for a small percentage of the time. Assuming that a music signal has a normal (Gaussian) amplitude distribution, the dissipation of a conventional BTL amplifier with the same output power is approximately 70% higher (see Fig.11).

The heatsink has to be designed for use with music signals. With such a heatsink, the thermal protection will disable the BTL mode when the junction temperature exceeds 150 °C. In this case, the output power is limited to 5 W per amplifier.

The gain of each amplifier is internally fixed at 26 dB. With the MODE pin, the device can be switched to the following modes:

- Standby with low standby current (<50 μ A)
- Mute condition, DC adjusted
- On, operation.

The information on pin 12 (selectable clip) determines at which distortion figures a clip detection signal will be generated at the clip output. A logic 0 applied to pin 12 will select clip detection at THD = 10%, a logic 1 selects THD = 2.5%. A logic 0 can be realised by connecting this pin to ground. A logic 1 can be realised by connecting it to V_{logic} (see Fig.7) or the pin can also be left open. Pin 12 may not be connected to V_P because its maximum input voltage is 18 V ($V_P > 18$ V under load dump conditions).

The device is fully protected against a short circuit of the output pins to ground and to the supply voltage. It is also protected against a short circuit of the loudspeaker and against high junction temperatures. In the event of a permanent short circuit to ground or the supply voltage, the output stage will be switched off, causing low dissipation. With a permanent short circuit of the loudspeaker, the output stage will be repeatedly switched on and off. In the 'on' condition, the duty cycle is low enough to prevent excessive dissipation.

To avoid plops during switching from 'mute' to 'on' or from 'on' to 'mute/standby' while an input signal is present, a built-in zero-crossing detector only allows switching at zero input voltage. However, when the supply voltage drops below 6 V (e.g. engine start), the circuit mutes immediately, avoiding clicks from the electronic circuit preceding the power amplifier.

The voltage of the SE electrolytic capacitor (pin 4) is kept at $0.5V_P$ by a voltage buffer (see Fig.1). The value of this capacitor has an important influence on the output power in SE mode. Especially at low signal frequencies, a high value is recommended to minimize dissipation.

The two diagnostic outputs (clip and diag) are open-collector outputs and require a pull-up resistor.

The clip output will be LOW when the THD of the output signal is higher than the selected clip level (10% or 2.5%).

The diagnostic output gives information:

- about short circuit protection:
 - When a short circuit (to ground or the supply voltage) occurs at the outputs (for at least 10 μ s), the output stages are switched off to prevent excessive dissipation. The outputs are switched on again approximately 50 ms after the short circuit is removed. During this short circuit condition, the protection pin is LOW.
 - When a short circuit occurs across the load (for at least 10 μ s), the output stages are switched off for approximately 50 ms. After this time, a check is made to see whether the short circuit is still present. The power dissipation in any short circuit condition is very low.
- during startup/shutdown, when the device is internally muted.
- temperature detection: This signal (junction temperature > 145°C) indicates that the temperature protection will become active. The temperature detection signal can be used to reduce the input signal and thus reduce the power dissipation.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _P	supply voltage	operating	–	18	V
		non-operating	–	30	V
		load dump; t _r > 2.5 ms	–	45	V
V _{P(sc)}	short-circuit safe voltage		–	18	V
V _{rp}	reverse polarity voltage		–	6	V
I _{ORM}	repetitive peak output current		–	4	A
P _{tot}	total power dissipation		–	60	W
T _{stg}	storage temperature		–55	+150	°C
T _{vj}	virtual junction temperature		–	150	°C
T _{amb}	ambient temperature		–40	–	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-c)}	thermal resistance from junction to case	see note 1	1.3	K/W
R _{th(j-a)}	thermal resistance from junction to ambient		40	K/W

Note

- The value of R_{th(c-h)} depends on the application (see Fig.3).

Heatsink design

There are two parameters that determine the size of the heatsink. The first is the rating for the virtual junction temperature and the second is the ambient temperature at which the amplifier must still deliver its full power in the BTL mode.

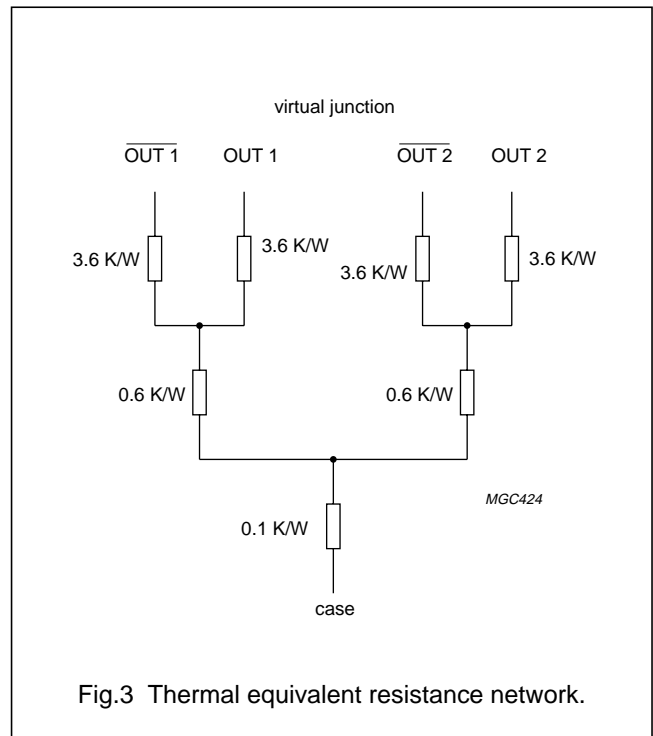
With a conventional BTL amplifier, the maximum power dissipation with a music-like signal (at each amplifier) will be approximately two times 6.5 W.

At a virtual junction temperature of 150 °C and a maximum ambient temperature of 65 °C, R_{th(vj-c)} = 1.3 K/W and R_{th(c-h)} = 0.2 K/W, the thermal resistance of the heatsink

should be: $\frac{150 - 65}{2 \times 6.5} - 1.3 - 0.2 = 5 \text{ K/W}$

Compared to a conventional BTL amplifier, the TDA1563Q has a higher efficiency. The thermal resistance of the

heatsink should be: $1.7 \left(\frac{145 - 65}{2 \times 6.5} \right) - 1.3 - 0.2 = 9 \text{ K/W}$



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DC CHARACTERISTICS

$V_P = 14.4$ V; $T_{amb} = 25$ °C; measured in Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage	note 1	6	14.4	18	V
$I_{q(tot)}$	total quiescent current	$R_L = \infty$	–	95	150	mA
I_{stb}	standby current		–	1	50	μA
V_C	average electrolytic capacitor voltage at pin 4		–	7.1	–	V
$ \Delta V_O $	DC output offset voltage	on state	–	–	100	mV
		mute state	–	–	100	mV
Mode select switch (see Fig.4)						
V_{ms}	voltage at mode select pin (pin 6)	standby condition	0	–	1	V
		mute condition	2	–	3	V
		operating condition	4	5	V_P	V
I_{ms}	switch current through pin 6	$V_{ms} = 5$ V	–	25	40	μA
Diagnostic						
V_{diag}	output voltage at diagnostic outputs (pins 14 and 15): protection/temperature and detection	during any fault condition	–	–	0.5	V
I_{diag}	current through pin 14 or 15	during any fault condition	2	–	–	mA
V_{SC}	input voltage at selectable clip pin (pin 12)	clip detect at THD = 10%	–	–	0.5	V
		clip detect at THD = 2.5%	1.5	–	18	V
Protection						
T_{pre}	prewarning temperature		–	145	–	°C
$T_{dis(BTL)}$	BTL disable temperature	note 2	–	150	–	°C

Notes

- The circuit is DC biased at $V_P = 6$ to 18 V and AC operating at $V_P = 8$ to 18 V.
- If the junction temperature exceeds 150 °C, the output power is limited to 5 W per channel.

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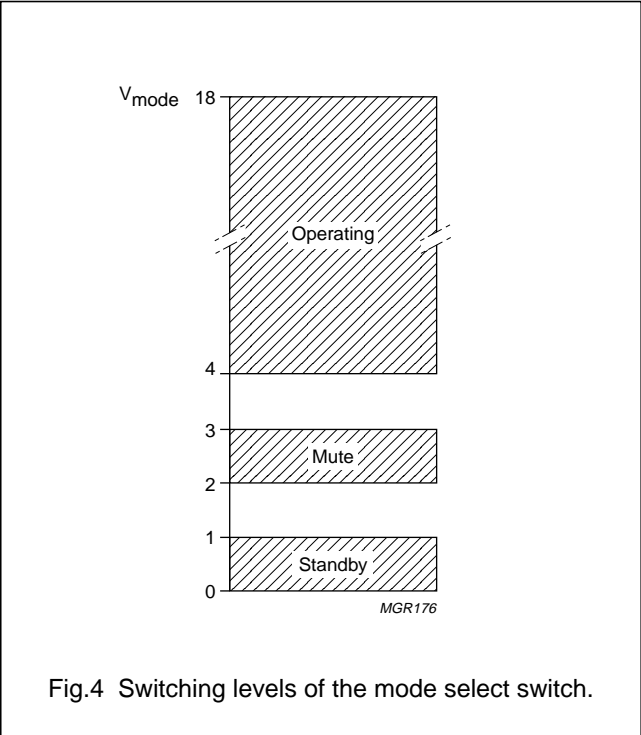


Fig.4 Switching levels of the mode select switch.

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AC CHARACTERISTICS

$V_P = 14.4$ V; $R_L = 4$ Ω ; CSE = 1000 μ F; $f = 1$ kHz; $T_{amb} = 25$ °C; measured in Fig.7; unless otherwise specified.

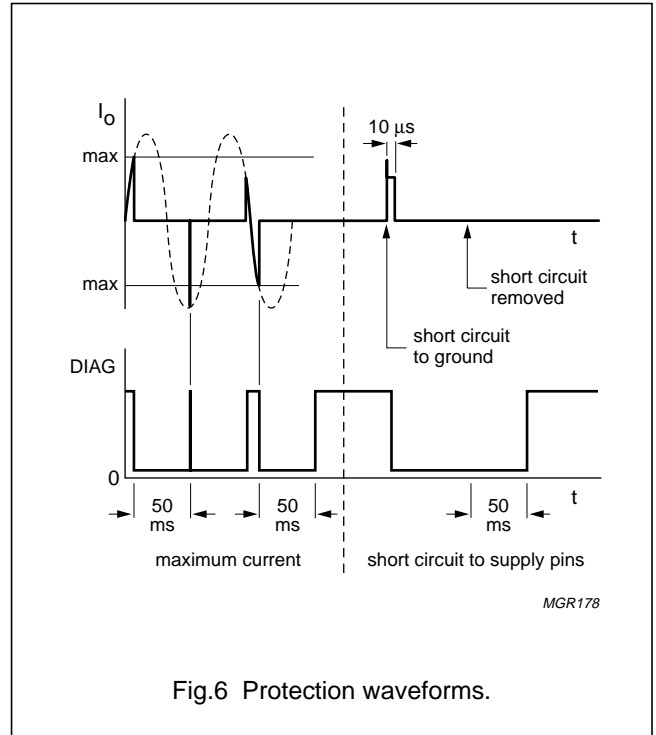
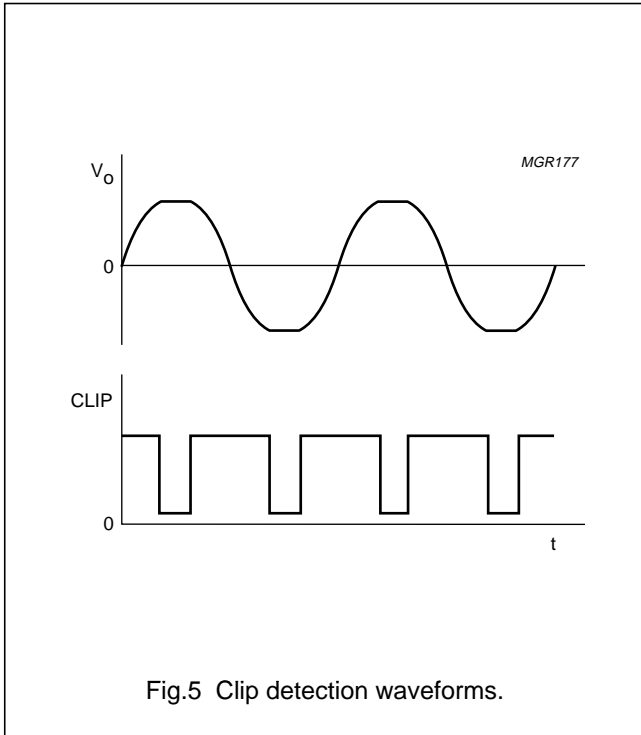
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 0.5%	15	19	–	W
		THD = 10%	23	25	–	W
		EIAJ	–	38	–	W
		$V_P = 13.2$ V; THD = 0.5%	–	16	–	W
		$V_P = 13.2$ V; THD = 10%	–	20	–	W
THD	total harmonic distortion	$P_o = 1$ W; note 1	–	0.1	–	%
P_d	dissipated power		see Figs 10 and 11			W
B_p	power bandwidth	THD = 1%; $P_o = -1$ dB with respect to 15 W	–	20 to 15 000	–	Hz
$f_{ro(l)}$	low frequency roll-off	-1 dB; note 2	–	25	–	Hz
$f_{ro(h)}$	high frequency roll-off	-1 dB	130	–	–	kHz
G_v	closed loop voltage gain	$P_o = 1$ W	25	26	27	dB
SVRR	supply voltage ripple rejection	$R_s = 0$ Ω ; $V_{ripple} = 2$ V (p-p) on/mute	45	65	–	dB
		standby; $f = 100$ Hz to 10 kHz	80	–	–	dB
CMRR	common mode rejection ratio	$R_s = 0$ Ω	–	80	–	dB
$ Z_i $	input impedance		90	120	150	k Ω
$ \Delta Z_i $	mismatch in input impedance		–	1	–	%
V_{SE-BTL}	SE to BTL switch voltage level	note 3	–	3	–	V
$ V_{o(mute)} $	output voltage mute (RMS value)	$V_i = 1$ V (RMS)	–	100	150	μ V
$V_{n(o)}$	noise output voltage	on; $R_s = 0$ Ω ; note 4	–	100	150	μ V
		on; $R_s = 10$ k Ω ; note 4	–	105	–	μ V
		mute; note 5	–	100	150	μ V
α_{CS}	channel separation	$R_s = 0$ Ω ; $P_o = 15$ W	40	70	–	dB
$ \Delta G_v $	channel unbalance		–	–	1	dB

Notes

1. The distortion is measured with a bandwidth of 10 Hz to 30 kHz.
2. Frequency response externally fixed (input capacitors determine low frequency roll-off).
3. The SE to BTL switch voltage level depends on V_P .
4. Noise output voltage measured with a bandwidth of 20 Hz to 20 kHz.
5. Noise output voltage is independent of R_s .

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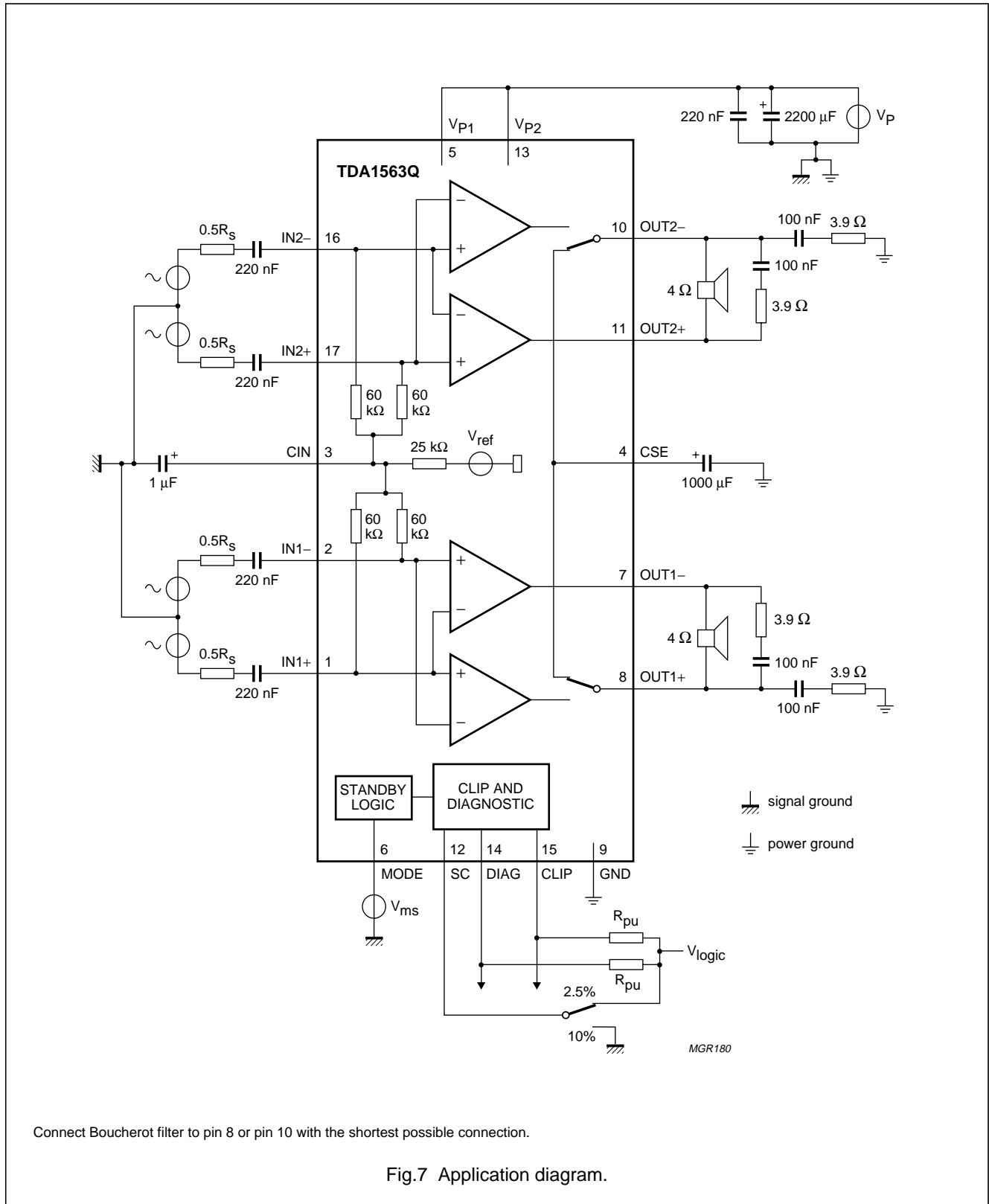
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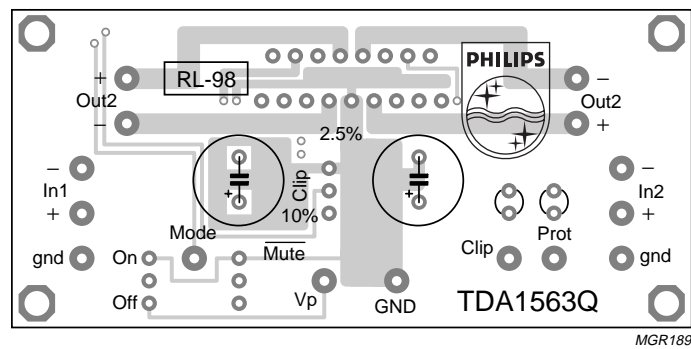
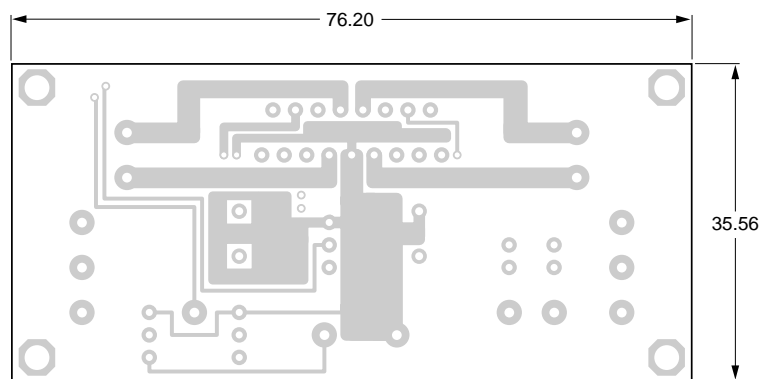
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TEST AND APPLICATION INFORMATION



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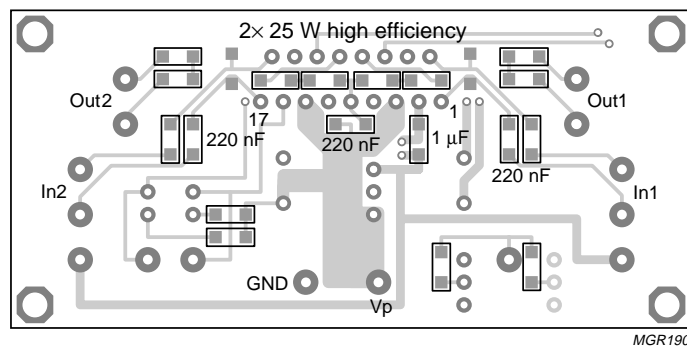
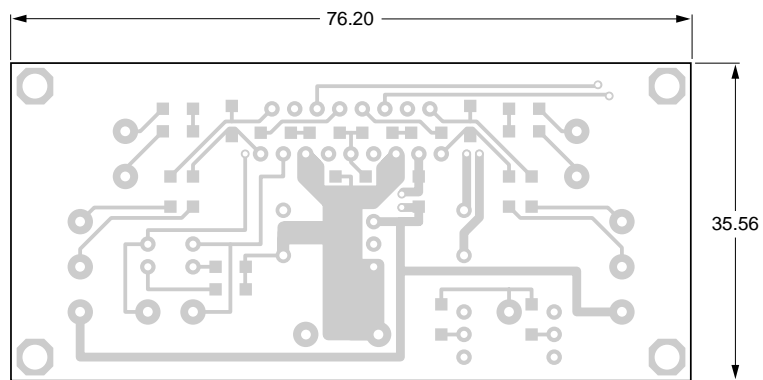


Dimensions in mm.

Fig.8 PCB layout (component side) for the application of Fig.7.

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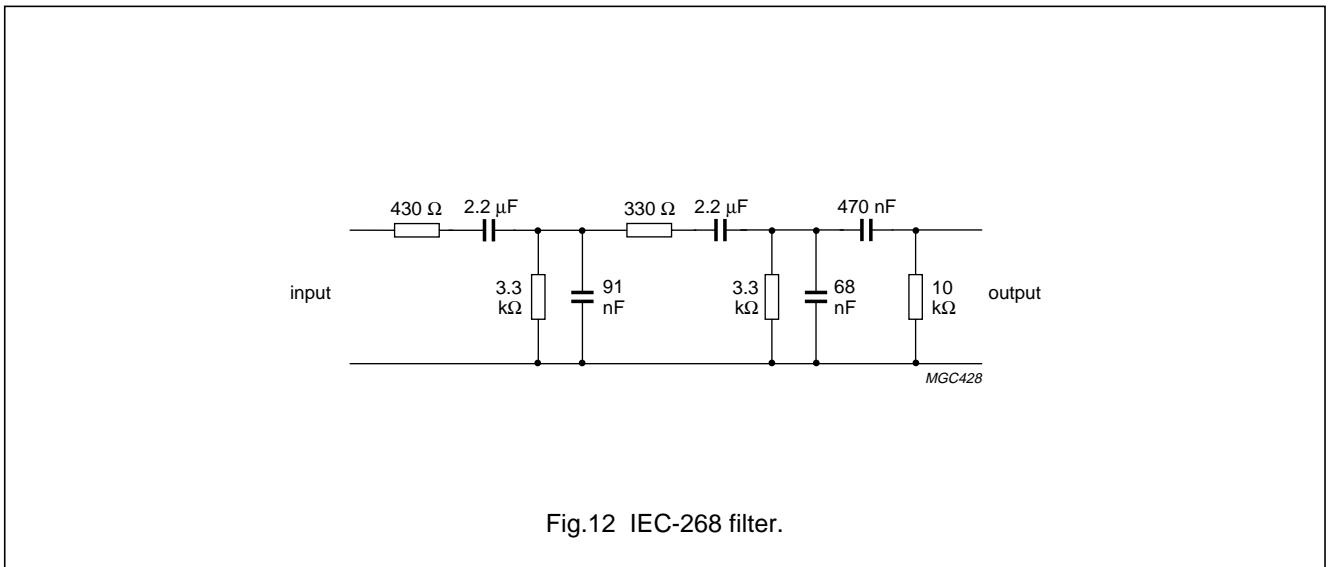
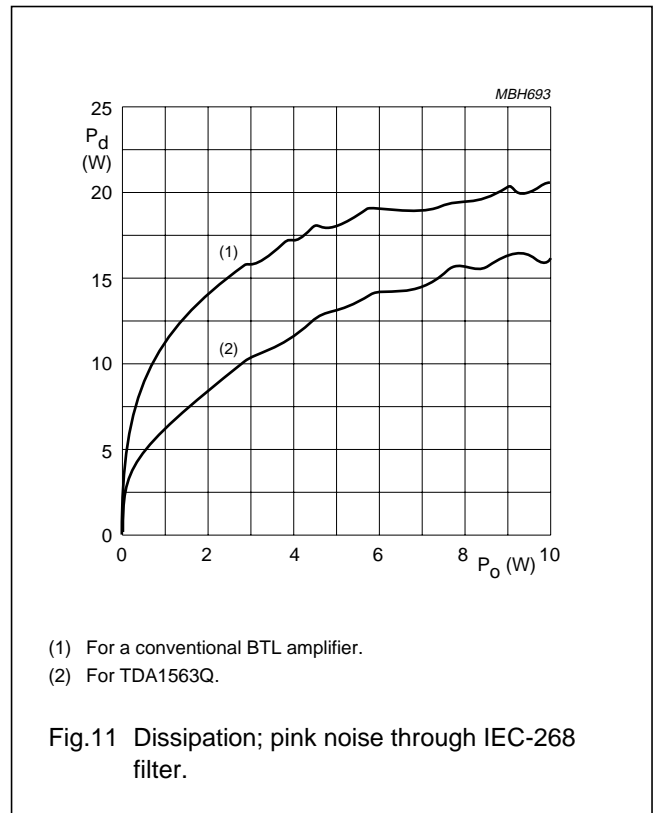
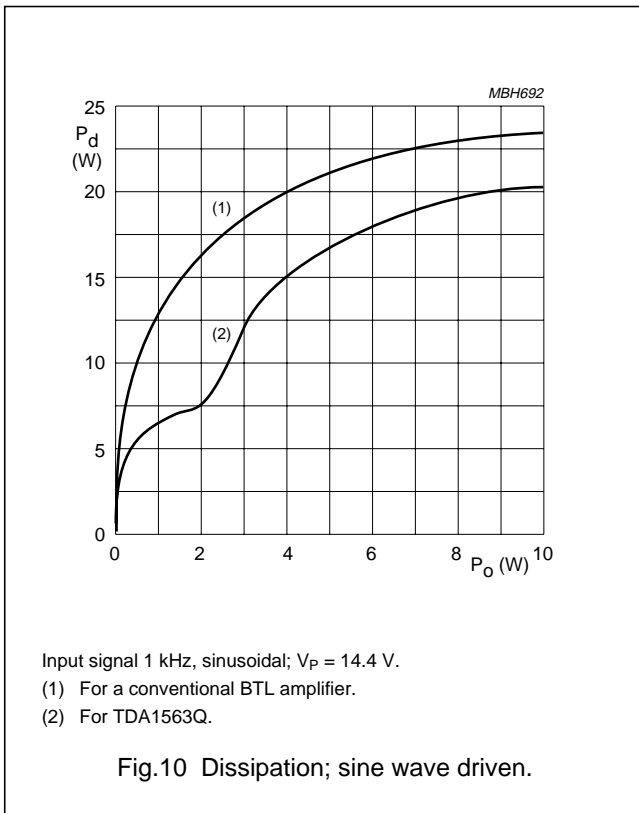


Dimensions in mm.

Fig.9 PCB layout (soldering side) for the application of Fig.7.

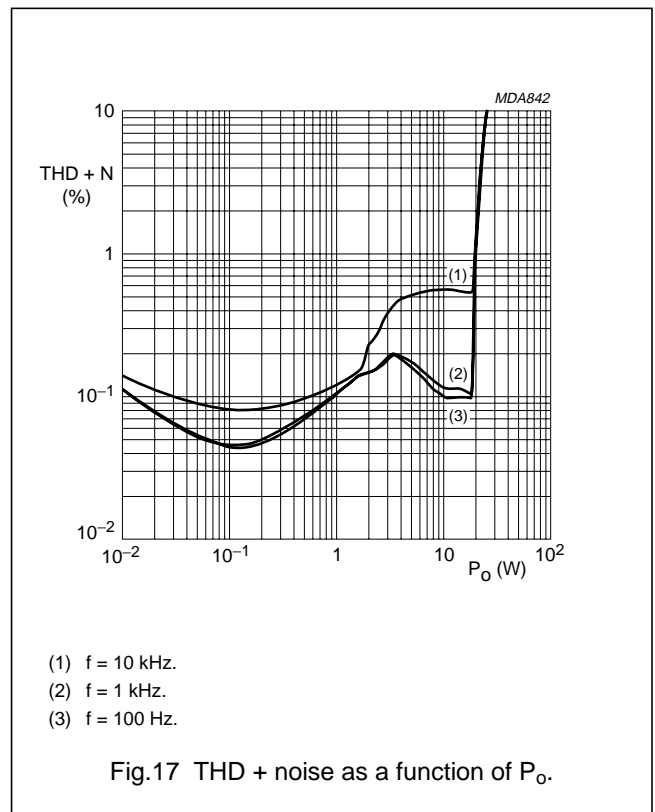
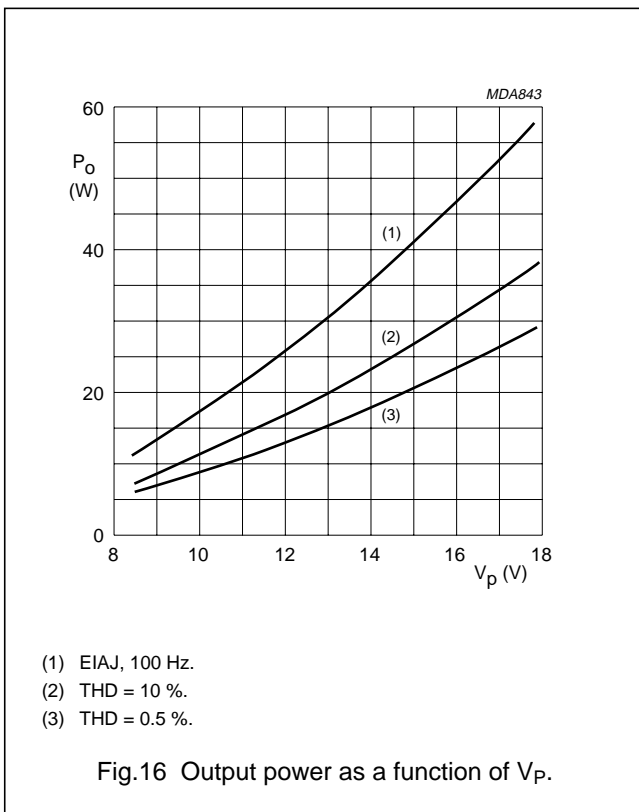
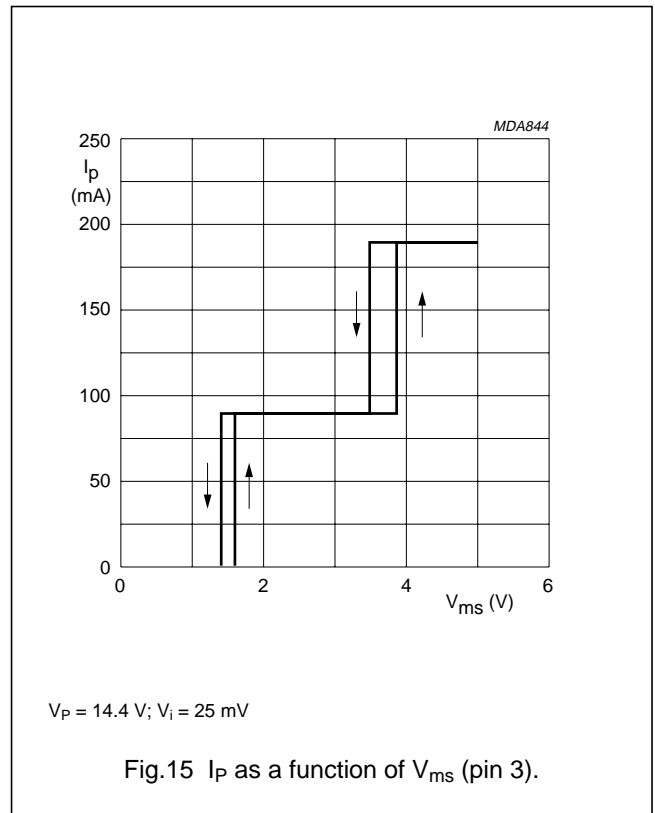
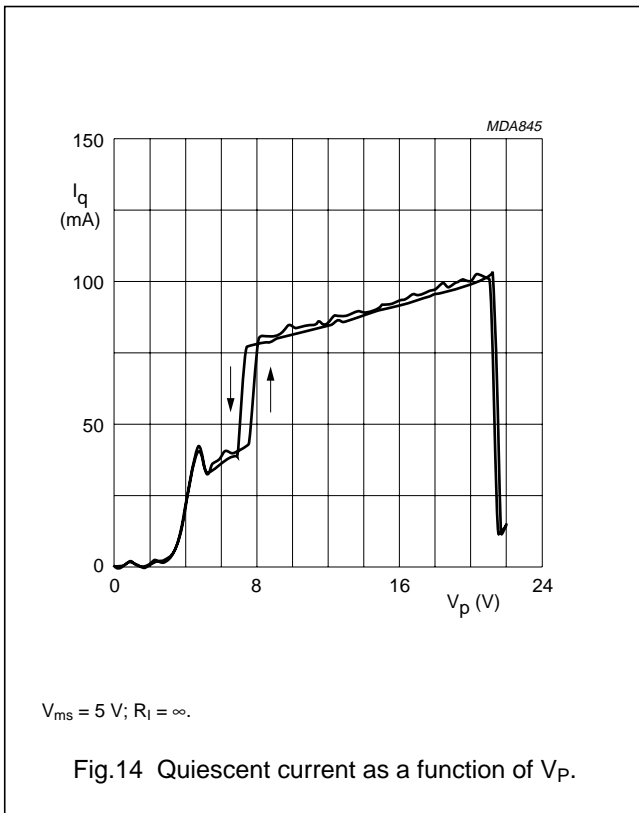
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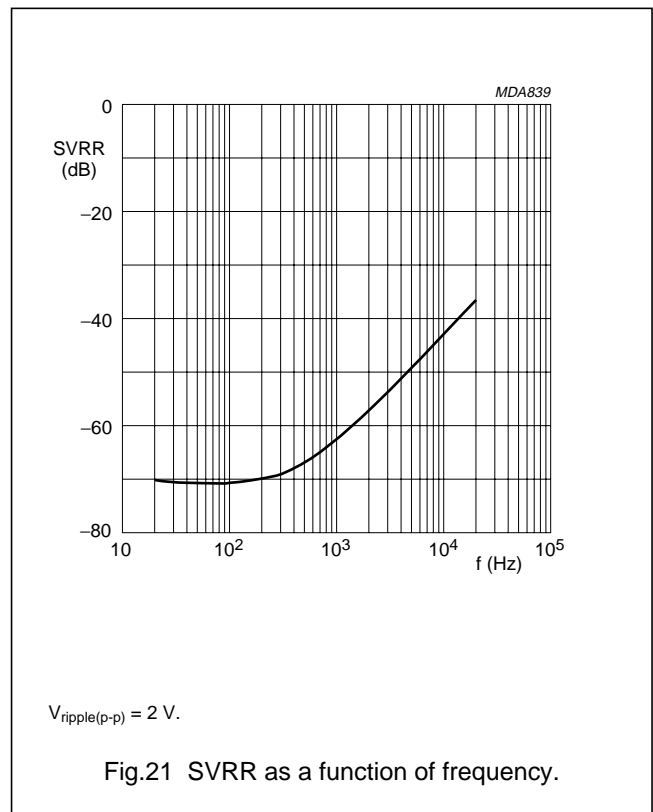
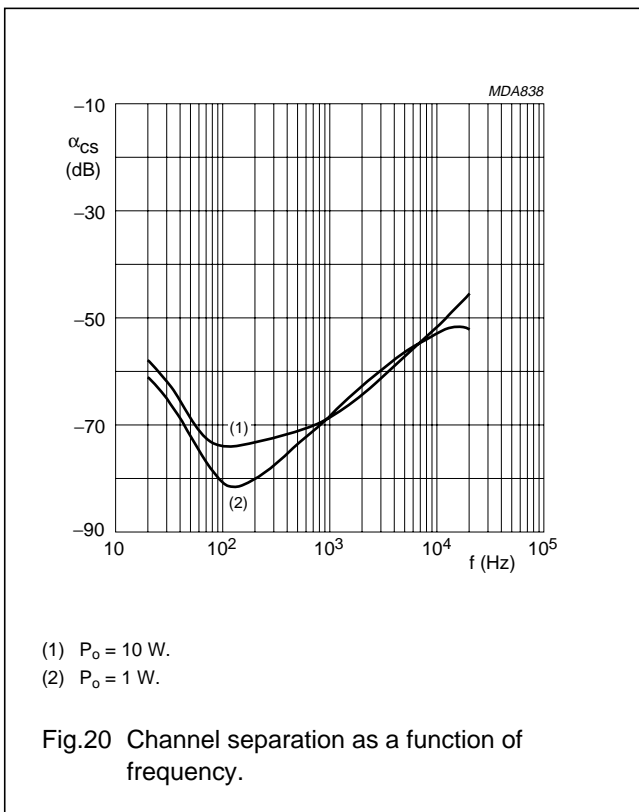
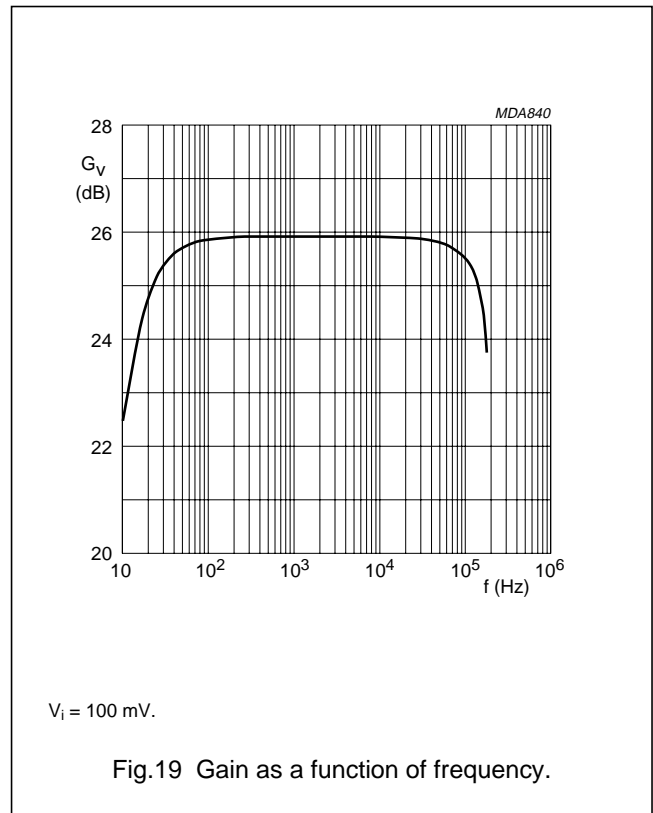
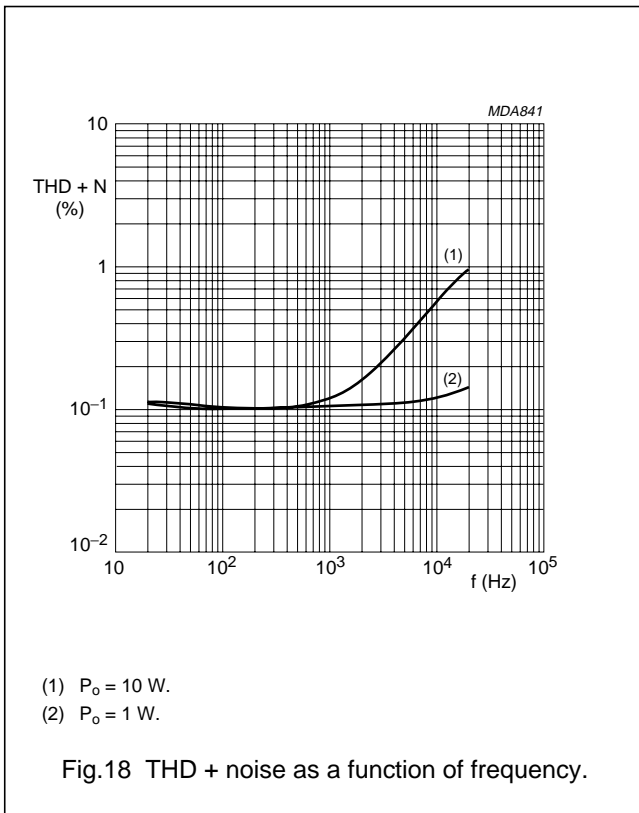
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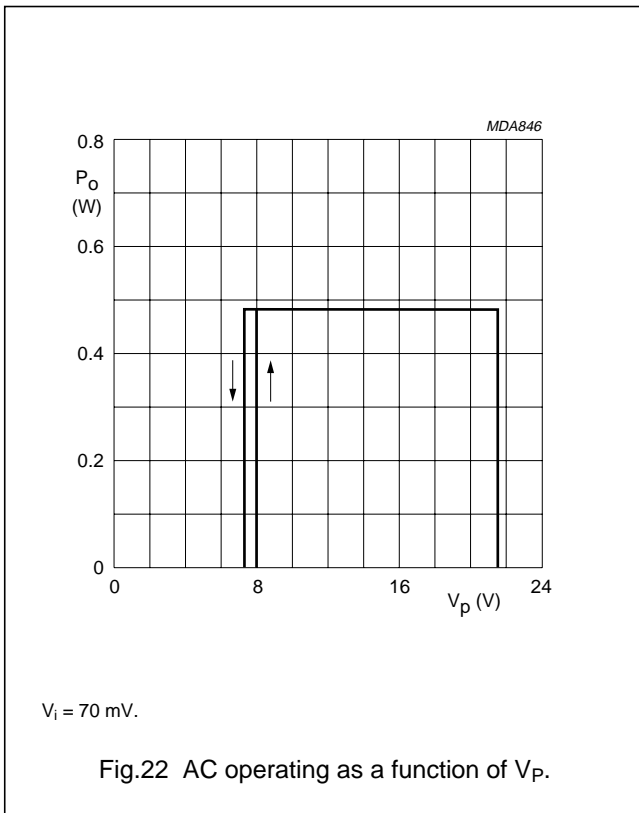
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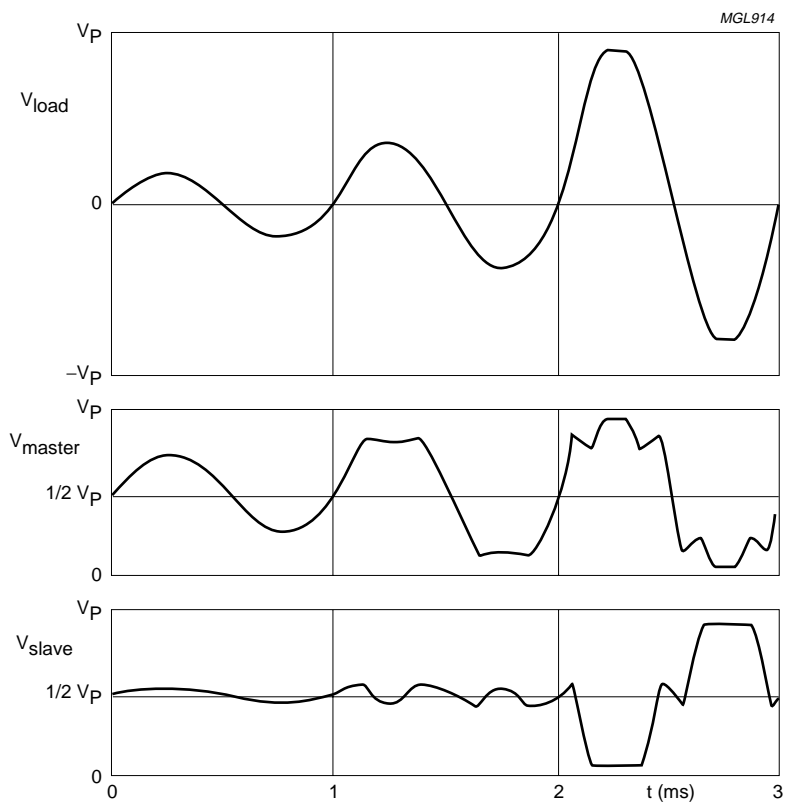
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See Fig.7:
 $V_{load} = V_7 - V_8$ or $V_{11} - V_{10}$
 $V_{master} = V_7$ or V_{11}
 $V_{slave} = V_8$ or V_{10}

Fig.23 Output waveforms.

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APPLICATION NOTES

Example of the TDA1563Q in a car radio system solution

The PCB shown here is used to demonstrate an audio system solution with Philips Semiconductors devices for car audio applications. The board includes the SAA7705H: a high-end CarDSP (Digital Signal Processor), the TDA3617J: a voltage regulator providing 9 V, 5 V and 3.3 V outputs, and two TDA1563Qs to provide four 25 W power outputs. A complete kit (application report, software and demo board) of this “car-audio chip-set demonstrator” is available.

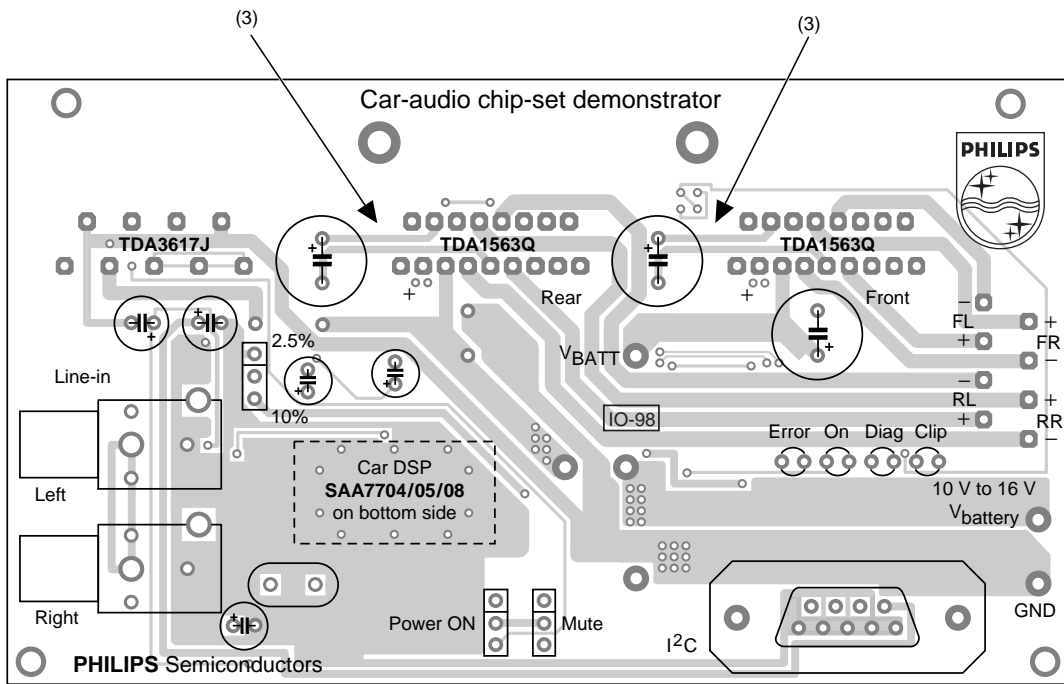
The TDA1563Q is a state of the art device, which is different to conventional amplifiers in power dissipation because it switches between SE mode and conventional BTL mode, depending on the required output voltage swing. As a result, the PCB layout is more critical than with conventional amplifiers.

NOTES AND LAYOUT DESIGN RECOMMENDATIONS

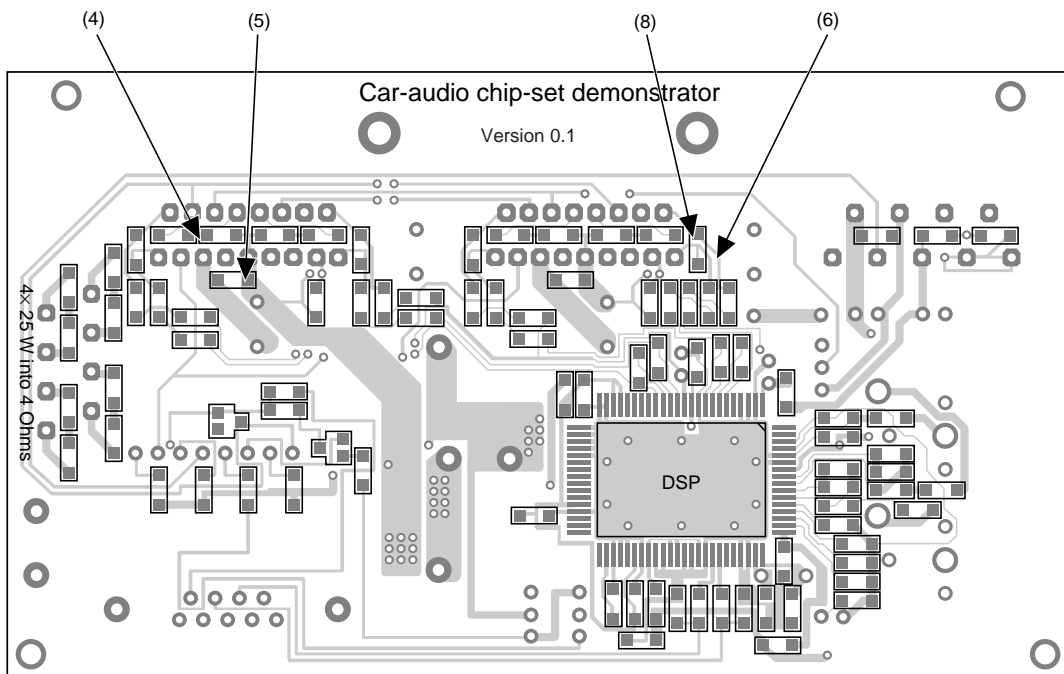
1. The TDA1563Q mutes automatically during switch-on and switch-off and suppresses biasing clicks coming from the CarDSP circuit preceding the power amplifier. Therefore, it is not necessary to use a plop reduction circuit for the CarDSP. To mute or to enlarge the mute time of the system, the voltage at the mode pin of the amplifiers should be kept between 2 V and 3 V.
2. The input reference capacitor at pin 3 is specified as 1 μF but has been increased to 10 μF to improve the switch-on plop performance of the amplifiers. By doing this, the minimum switch-on time increases from standby, via internal mute, to operating from 150 ms to 600 ms.
3. It is important that the copper tracks to and from the electrolytic capacitors (SE capacitors and supply capacitors) are close together. Because of the switching principle, switching currents flow here. Combining electrolytic capacitors in a 4-channel application is not recommended.
4. Filters at the outputs are necessary for stability reasons. The filters at output pins 8 and 10 to ground should be connected as close as possible to the device (see layout of PCB).
5. Connect the supply decoupling capacitors of 220 nF as closely as possible to the TDA1563Qs.
6. Place the tracks of the differential inputs as close together as possible. If disturbances are injected at the inputs, they will be amplified 20 times. Oscillation may occur if this is not done properly.
7. The SE line output signal of the CarDSP here is offered as a quasi differential input signal to the amplifiers by splitting the 100 Ω unbalance series resistance into two 47 Ω balanced series resistances. The return track from the minus inputs of the amplifiers are not connected to ground (plane) but to the line out reference voltage of the CarDSP, VrefDA.
8. The output signal of the CarDSP needs an additional 1st order filter. This is done by the two balanced series resistances of 47 Ω (see note 7) and a ceramic capacitor of 10 nF. The best position to place these 10 nF capacitors is directly on the input pins of the amplifiers. Now, any high frequency disturbance at the inputs of the amplifiers will be rejected.
9. Only the area underneath the CarDSP is a ground plane. A ground plane is necessary in PCB areas where high frequency digital noise occurs. The audio outputs are low frequency signals. For these outputs, it is better to use two tracks (feed and return) as closely as possible to each other to make the disturbances common mode. The amplifiers have differential inputs with a very high common mode rejection.
10. The ground pin of the voltage regulator is the reference for the regulator outputs. This ground reference should be connected to the ground plane of the CarDSP by one single track. The ground plane of the CarDSP may not be connected to “another” ground by a second connection.
11. Prevent power currents from flowing through the ground connection between CarDSP and voltage regulator. The currents in the ground from the amplifiers are directly returned to the ground pin of the demo board. By doing this so, no ground interference between the components will occur.

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Top copper layer



Bottom copper layer

MGS827

Fig.24 PCB layout.

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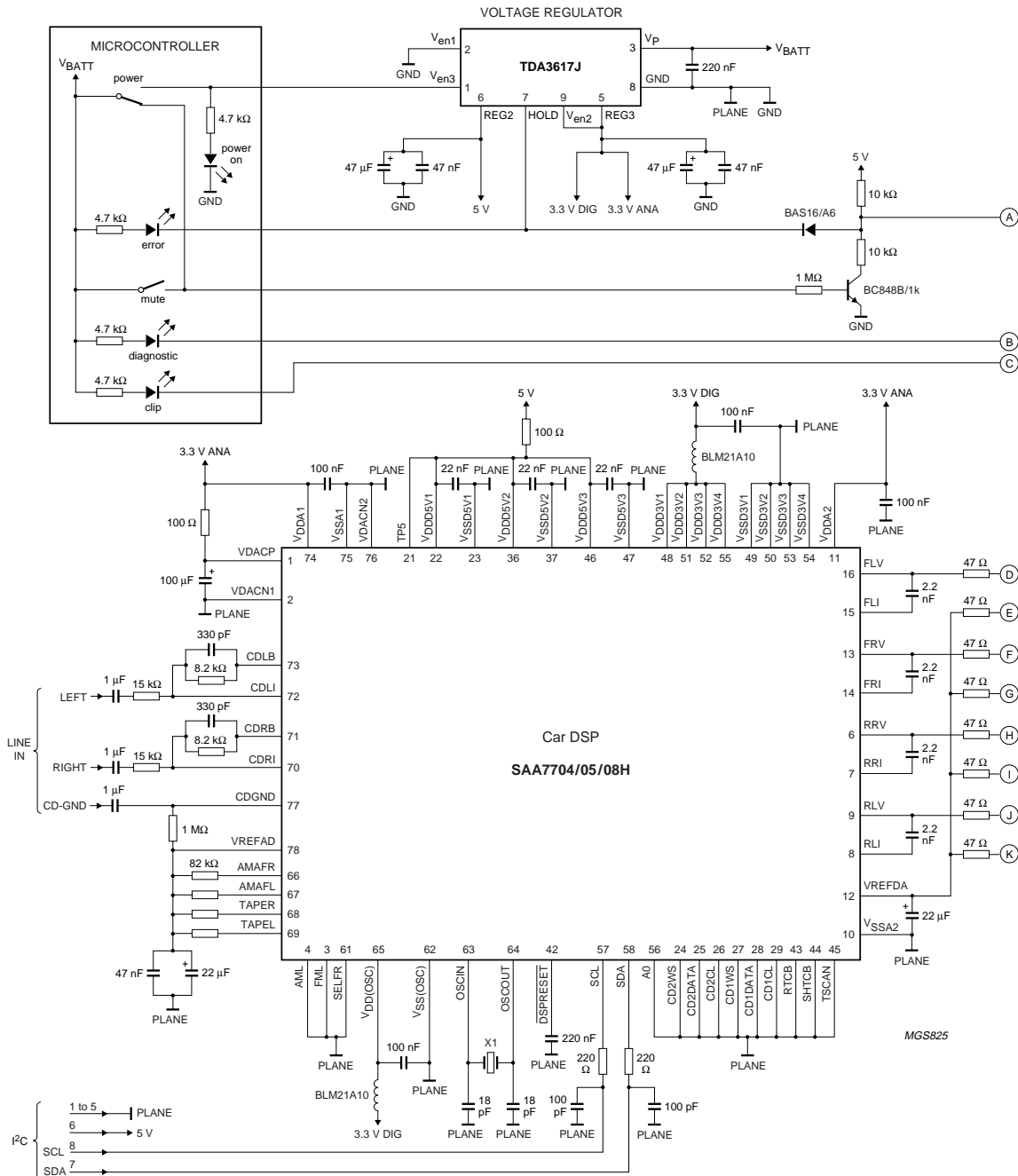


Fig.25 Car-audio chip-set demonstrator (continued in Fig.26).

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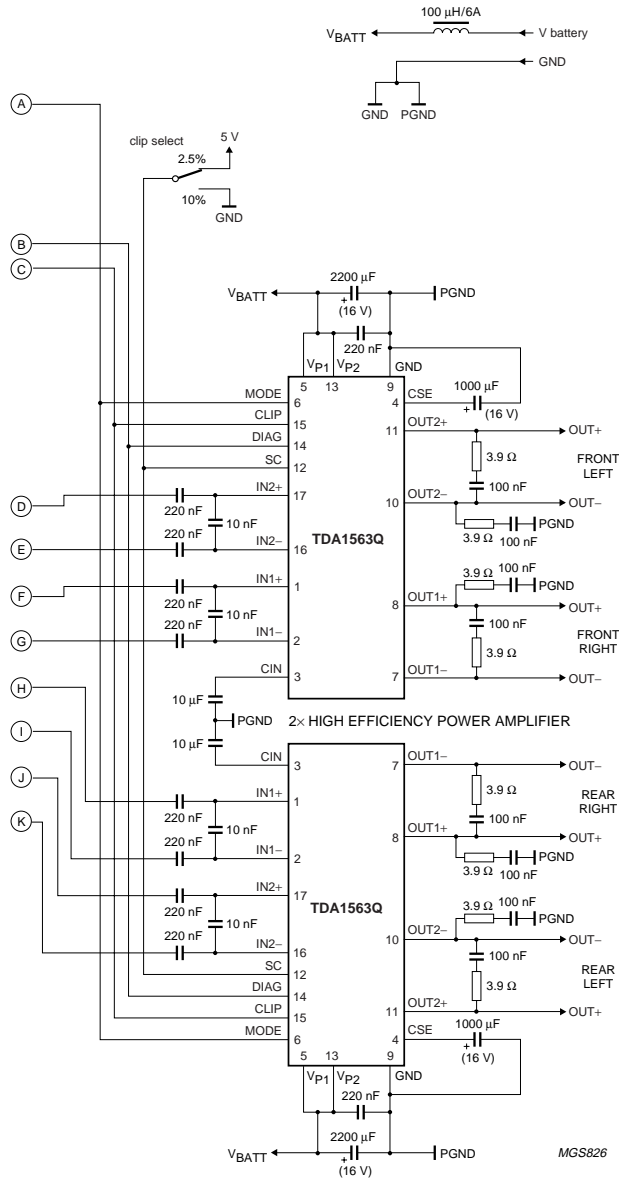


Fig.26 Car-audio chip-set demonstrator (continued from Fig.25).

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Advantages of high efficiency

- Power conversion improvement (power supply)**
 Usually, the fact that the reduction of dissipation is directly related to supply current reduction is neglected. One advantage is less voltage drop in the whole supply chain. Another advantage is less stress for the coil in the supply line. Even the adapter or supply circuit remains cooler than before as a result of the reduced heat dissipation in the whole chain because more supply current will be converted to output power.
- Power dissipation reduction**
 This is the best known advantage of high efficiency amplifiers.
- Heatsink size reduction**
 The heatsink size of a conventional amplifier may be reduced by approximately 50% at $V_P = 14.4$ V when the TDA1563Q is used. In this case, the maximum heatsink temperature will remain the same.
- Heatsink temperature reduction**
 The power dissipation and the thermal resistance of the heatsink determine the heatsink temperature rise. When the same heatsink size is used as in a conventional amplifier, the maximum heatsink temperature decreases and also the maximum junction temperature, which extends the life of this semiconductor device. The maximum dissipation with music-like input signals decreases by 40%.

It is clear that the use of the TDA1563Q saves a significant amount of energy. The maximum supply current decreases by approximately 32%, which reduces the dissipation in the amplifier as well in the whole supply chain. The TDA1563Q allows a heatsink size reduction of approximately 50% or a heatsink temperature decrease of 40% when the heatsink size is not changed.

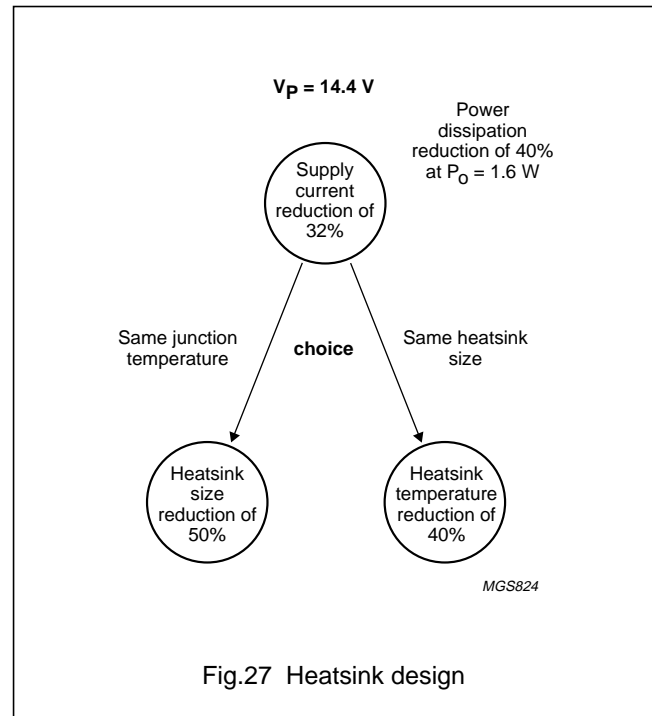


Fig.27 Heatsink design

Advantage of the concept used by the TDA1563Q

The TDA1563Q is highly efficient under all conditions, because it uses a SE capacitor to create a non-dissipating half supply voltage. Other concepts rely on both input signals being the same in amplitude and phase. With the concept of an SE capacitor, it does not matter what kind of signal processing is done on the input signals. For example, amplitude difference, phase shift or delays between both input signals, or other DSP processing, have no impact on the efficiency.

2 × 25 W high efficiency car radio power amplifier

TDA1563Q

INTERNAL PIN CONFIGURATIONS

PIN	NAME	EQUIVALENT CIRCUIT
1, 2, 16, 17 and 3	IN1+, IN1-, IN2-, IN2+ and CIN	
4	C _{SE}	
6	MODE	
7, 11	OUT1-, OUT2+	

2 × 25 W high efficiency car radio power amplifier

TDA1563Q

PIN	NAME	EQUIVALENT CIRCUIT
8, 10	OUT1+, OUT2-	
12	SC	
14, 15	PROT, CLIP	

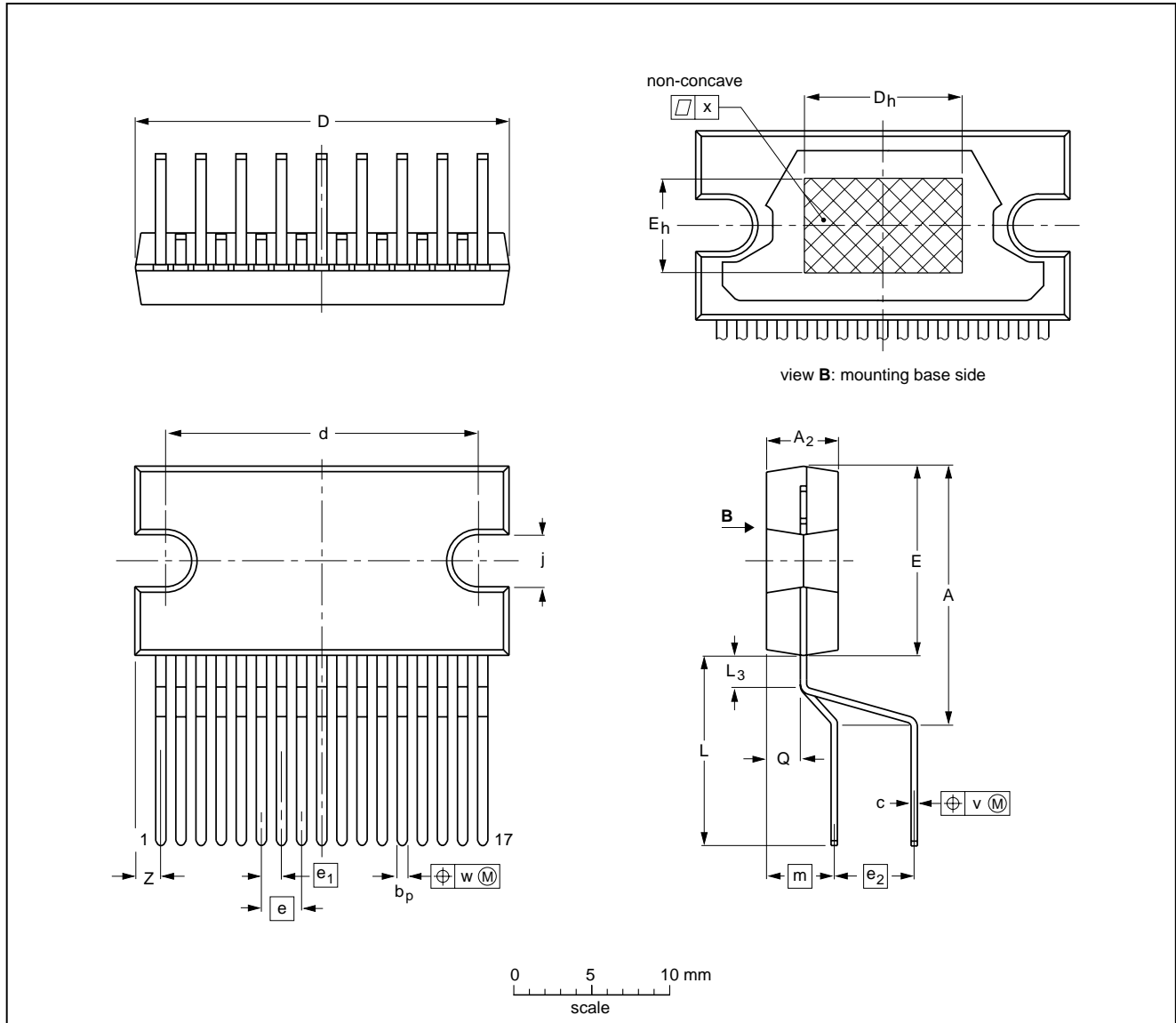
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PACKAGE OUTLINE

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)

SOT243-1



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₂	b _p	c	D ⁽¹⁾	d	D _h	E ⁽¹⁾	e	e ₁	e ₂	E _h	j	L	L ₃	m	Q	v	w	x	Z ⁽¹⁾
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						97-12-16 99-12-17

2 × 25 W high efficiency car radio power amplifier

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SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable ⁽¹⁾

Note

- For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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2 × 25 W high efficiency car radio power amplifier

TDA1563Q

NOTES

2 × 25 W high efficiency car radio power amplifier

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**2 × 25 W high efficiency car radio power
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Printed in The Netherlands

753503/25/02/pp32

Date of release: 2000 Feb 09

Document order number: 9397 750 06309

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