

TDA2591/3

LINE OSCILLATOR COMBINATION

The TDA2591 and TDA2593 are integrated line oscillator circuits for colour television receivers using thyristor or transistor line deflection output stages.

The circuits incorporate a line oscillator which is based on the threshold switching principle, a line deflection output stage capable of direct drive of thyristor deflection circuits, phase comparison between the oscillator voltage and both the sync pulse and line flyback pulse. Also included on the chip is a switch for changing the filter characteristic and the gate circuit when used for VCR.

The TDA2593 generates a sandcastle pulse (at pin 7) suitable for use with the TDA2532.

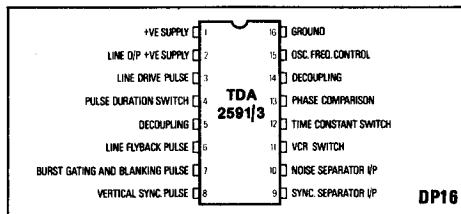


Fig.1 Pin connections (top view)

FEATURES

- Coincidence Detector
- Sync Separator
- Noise Separator
- Vertical Sync Separator
- Colour Burst Keying
- Line Flyback Pulse Generator
- Output Pulse Phase Shifter
- Output Pulse Duration Switching
- Sync Gating Pulse Generator
- Low Supply Voltage Protection

ABSOLUTE MAXIMUM RATINGS

Voltages

Supply pin 1 (when supplied by the IC)	13.2V
Supply pin 2	18V
Pin 4	0V to 13.2V
Pin 9	-6V to +6V
Pin 10	-6V to +6V
Pin 11	0V to 13.2V

Currents

Pin 2	400mA peak	} 650mA thyristor drive only
Pin 3	400mA peak	
Pin 4	1mA peak	
Pin 6	10mA peak	
Pin 7	10mA peak	
Pin 11	2mA peak	

Power dissipation

Total power dissipation	800mW
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Temperature

Storage temperature	-55°C to +125°C
Operating ambient temperature	-10°C to +60°C

QUICK REFERENCE DATA

- Supply Voltage (pin 1) 12V typ.
- Supply Current 30mA typ.
- Sync Separator Input (pin 9) 3V p-p typ.
- Pulse Duration Switch Input (pin 4)
 - at $t = 7\mu\text{s}$ 9.4V to V_1
 - at $t = 14\mu\text{s} + t_d$ 0V to 4V
- VCR Switch ON (pin 11) 0V to 1.5V and 9V to V_1

Output signal

- Vertical Sync Pulse (pin 8) 11V p-p (typ.)
- Burst Gating Pulse (pin 7) 11V p-p (typ.)
- Line Drive Pulse (pin 3) 10.5V p-p (typ.)

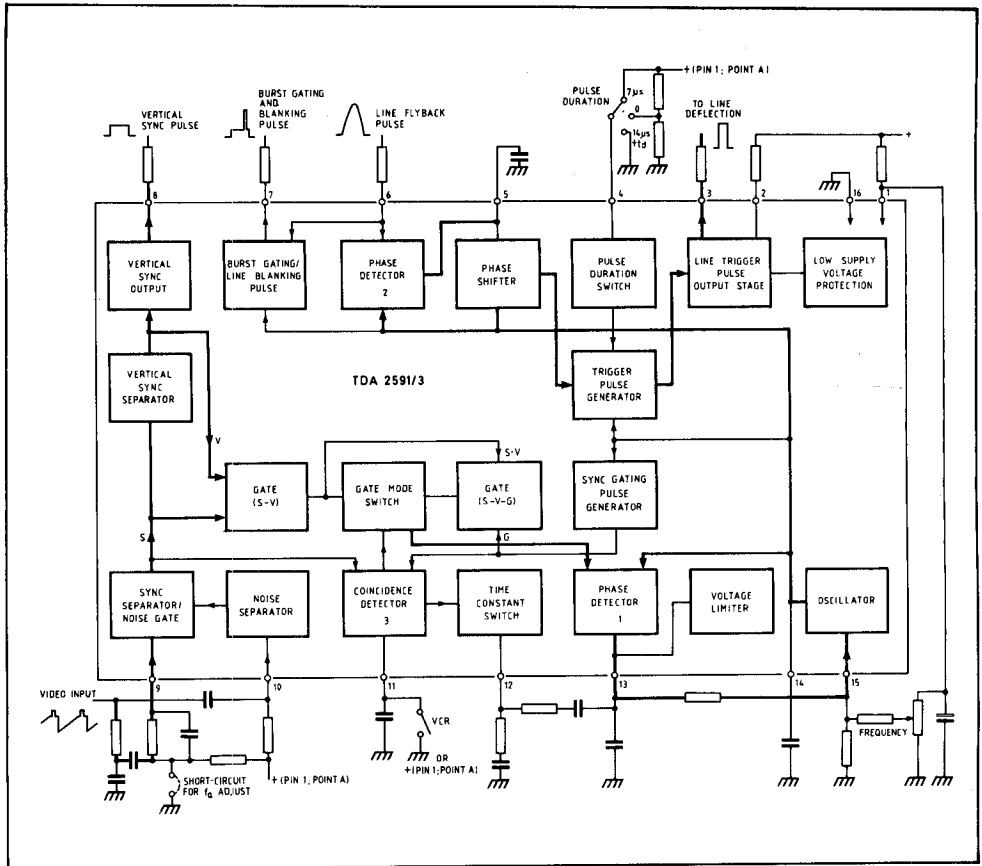


Fig. 2 TDA2591/3 block diagram

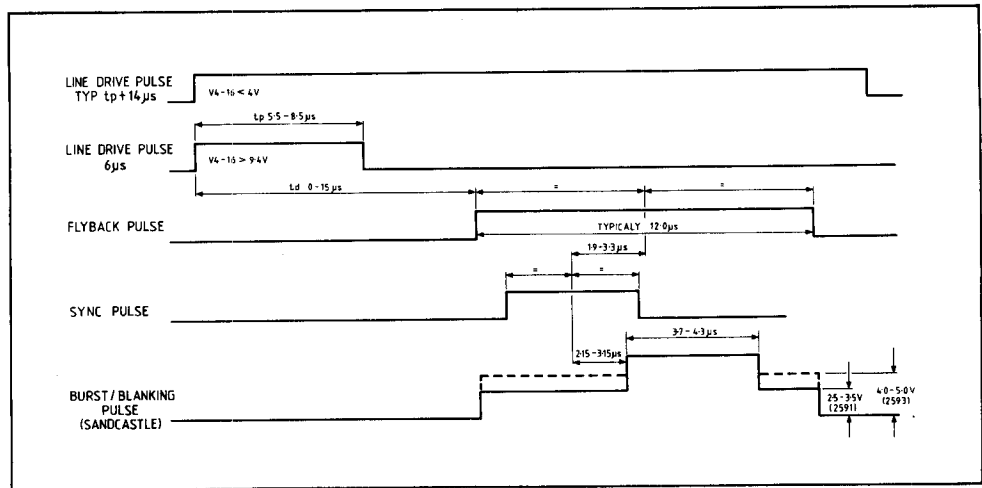


Fig. 3 TDA2591/3 timing relations

ELECTRICAL CHARACTERISTICS**Test conditions (unless otherwise stated):**Supply voltage, $V_1 = 12V$ $T_{amb} = +25^{\circ}C$

Refer to timing diagram, Fig. 3 and Application circuit, Fig. 4

Voltages are referred to pin 6

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Sync separator	9		0.8		V	$V_9 = -5V$
Input switching voltage		5		100	μA	
Input keying current				1	μA	
Input blocking current				5	μA	
Noise separator	10		1.4		V	$V_{10} = -5V$
Input switching voltage		5		100	μA	
Input keying current			150		μA	
Input blocking current				1	μA	
Line flyback pulse	6		1.4		μA	
Input current		10			V	
Input switching voltage					V	
Input limiting voltage		-0.7		+1.4	V	
Input resistance		400			Ω	
Pulse duration switch	4		9.4	V_1	V	$t = 7\mu s$
Input voltage		200			μA	$t = 14\mu s + t_d$
Input current		0		4.0	V	
Input voltage		200			μA	$t = 0, V_3 = 0$
Input current		5.4		6.5	V	
Input voltage (input open)				0	μA	See note 1
VCR Switching	11		0	1.5	V	See note 2
Input voltage (typical range)		9		V_1	V	
Input current		200			μA	$V_{11} = 0V$ to $1.5V$ $V_{11} = 9V$ to V_1
Output current		1		2	mA	
Vertical sync pulse (positive going)	8		11		V_{p-p}	
Output voltage		10			k Ω	
Output resistance		2				
Burst gating pulse (positive-going)	7		11		V_{p-p}	
Output voltage		10			Ω	
Output resistance		400				
Blanking pulse	7		2.5	3.5	V_{p-p}	
Output voltage (typical range) 2591		4.0		5.0	V_{p-p}	
Output voltage (typical range) 2593			400		Ω	
Output resistance						
Line drive pulse (positive going)	3		10.5		V_{p-p}	
Output voltage			100		mA	
Output current (average value)				2.5	Ω	
Output resistance for leading edge of line pulse				20	Ω	
Output resistance for trailing edge of line pulse						
Oscillator	14		4.4		V	
Threshold voltage low level			7.6		V	
Threshold voltage high level			0.47		mA	
Discharge current						
Phase comparison (ϕ_1: sync pulse/oscillator)	13		3.8	8.2	V	$V_{13} = 4V$ to $8V$ $V_{13} = 4V$ to $8V$ $V_{13} < 3.8V$ or $> 8.2V$
Control voltage range (typ)		1.9	2.1	2.3	mAp-p	
Control current				1	μA	
Output blocking current						
Output resistance			High (see note 3) Low (see note 4)			
Time constant switch	12		6		V	$V_{11} = 2.5V$ to $7V$ $V_{11} < 1.5V$ or $> 9V$
Output voltage				1	mA	
Output current			100		Ω	
Output resistance			60		k Ω	

ELECTRICAL CHARACTERISTICS (Contd.)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Coincidence detector (θ_3)	11	0.5		6	V	
Output voltage typical range						
Output current:			0.1		mAp-p	
without coincidence			0.5		mAp-p	
with coincidence						
Phase comparison (θ_2: oscillator/line flyback pulse)	5	5.4		7.6	V	$V_5 = 5.4V$ to $7.6V$
Control voltage range (typ)			1		mAp-p	$V_5 < 5.4V$ or $> 7.6V$
Control current		High	(see note 3)		k Ω	
Output resistance			8		k Ω	
Input current at blocked phase detector				5	μA	$V_5 = 5.4V$ to $7.6V$
Applications (see Fig. 4)	9					
Sync separator						
Input voltage (negative video signal):	1	3	7		Vp-p	
Input keying current range	5		100		μA	
Noise gating	10					
Input voltage	1	3	7		Vp-p	
Input keying current range	5		100		μA	
Superimposed noise voltage			7		Vp-p	
Vertical sync pulse separator						
Delay between leading edge of input and output signal, t_{on}			12		μs	
Delay between trailing edge of input and output signal, t_{off}				t_{on}	μs	
Output voltage	8	11			Vp-p	
Output resistance	8	2			k Ω	
Oscillator						
Frequency: free running		15.625			kHz	$C_{14} = 4.7nF$, $R_{15} = 10k\Omega$
Spread of frequency, $\Delta f_o/f_o$			± 5		%	See note 5
Frequency control sensitivity, $\Delta f_o/\Delta I_{15}$		31			Hz/ μA	
Adjustment range of network in Fig. 2		± 10			%	
Influence of supply voltage on frequency $\Delta f_o/f_o$				± 0.05		See note 5, $V_1 = 12V$
$\frac{\Delta V/V_{nom}}{\Delta V/V_{nom}}$						
Change of frequency when V_1 drops to 5V				± 10	%	See note 5
Temperature coefficient of oscillator frequency per $^{\circ}C$				$\pm 10^{-4}$		
Phase comparison (θ_1: sync pulse/oscillator)						
Control sensitivity			2		kHz/ μs	
Catching and holding range (82k Ω between pins 13 and 15)		± 780			Hz	$R_{13-15} = 82k\Omega$
Spread of catching and holding range		± 10			%	See note 5
Phase comparison (θ_2: oscillator/line flyback pulse)						
Permissible delay between leading edge of output pulse and leading edge of flyback pulse, Δt_d	0		15		μs	
Static control error, t_d/t_d			0.2		%	
Overall phase relation See Note 6						
Phase relation between middle of sync pulse and the middle of the flyback pulse, t		2.6			μs	
Tolerance of phase relation Δt			0.7		μs	
Adjustment sensitivity of overall phase relation	5					
caused by: adjustment voltage $\Delta V_5/\Delta t$			0.1		V/ μs	
adjustment current, $\Delta I_5/\Delta t$		30			$\mu A/\mu s$	

