CD54HC221, CD74HC221, CD74HCT221

Data sheet acquired from Harris Semiconductor
SCHS166F

November 1997 - Revised October 2003

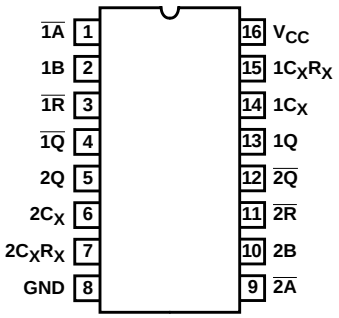
High-Speed CMOS Logic
Dual Monostable Multivibrator with Reset

Features

- **Overriding RESET Terminates Output Pulse**
- **Triggering from the Leading or Trailing Edge**
- **Q and $\overline{Q}$ Buffered Outputs**
- **Separate Resets**
- **Wide Range of Output-Pulse Widths**
- **Schmitt Trigger on B Inputs**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^{o}C to 125^{o}C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Pinout

CD54HC221
(CERDIP)
CD74HC221
(PDIP, SOIC, SOP, TSSOP)
CD74HCT221
(PDIP, SOIC)
TOP VIEW



Description

The ’HC221 and CD74HCT221 are dual monostable multivibrators with reset. An external resistor (R_X) and an external capacitor (C_X) control the timing and the accuracy for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. Pulse triggering on the B input occurs at a particular voltage level and is not related to the rise and fall time of the trigger pulse.

Once triggered, the outputs are independent of further trigger inputs on $\overline{A}$ and B. The output pulse can be terminated by a LOW level on the Reset ($\overline{R}$) pin. Trailing Edge triggering ($\overline{A}$) and leading-edge-triggering (B) inputs are provided for triggering from either edge of the input pulse. On power up, the IC is reset. If either Mono is not used each input (on the unused device) must be terminated either high or low.

The minimum value of external resistance, R_X, is typically 500Ω. The minimum value of external capacitance, C_X, is 0pF. The calculation for the pulse width is $t_W = 0.7\ R_X C_X$ at V_{CC} = 4.5V.

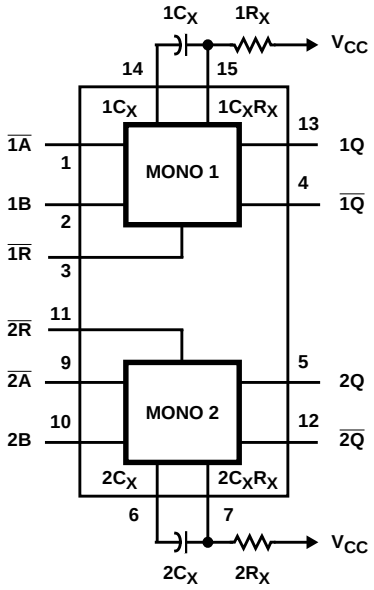
Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE
CD54HC221F3A	-55 to 125	16 Ld CERDIP
CD74HC221E	-55 to 125	16 Ld PDIP
CD74HC221M	-55 to 125	16 Ld SOIC
CD74HC221MT	-55 to 125	16 Ld SOIC
CD74HC221M96	-55 to 125	16 Ld SOIC
CD74HC221NSR	-55 to 125	16 Ld SOP
CD74HC221PW	-55 to 125	16 Ld TSSOP
CD74HC221PWR	-55 to 125	16 Ld TSSOP
CD74HC221PWT	-55 to 125	16 Ld TSSOP
CD74HCT221E	-55 to 125	16 Ld PDIP
CD74HCT221M	-55 to 125	16 Ld SOIC
CD74HCT221MT	-55 to 125	16 Ld SOIC
CD74HCT221M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram



TRUTH TABLE

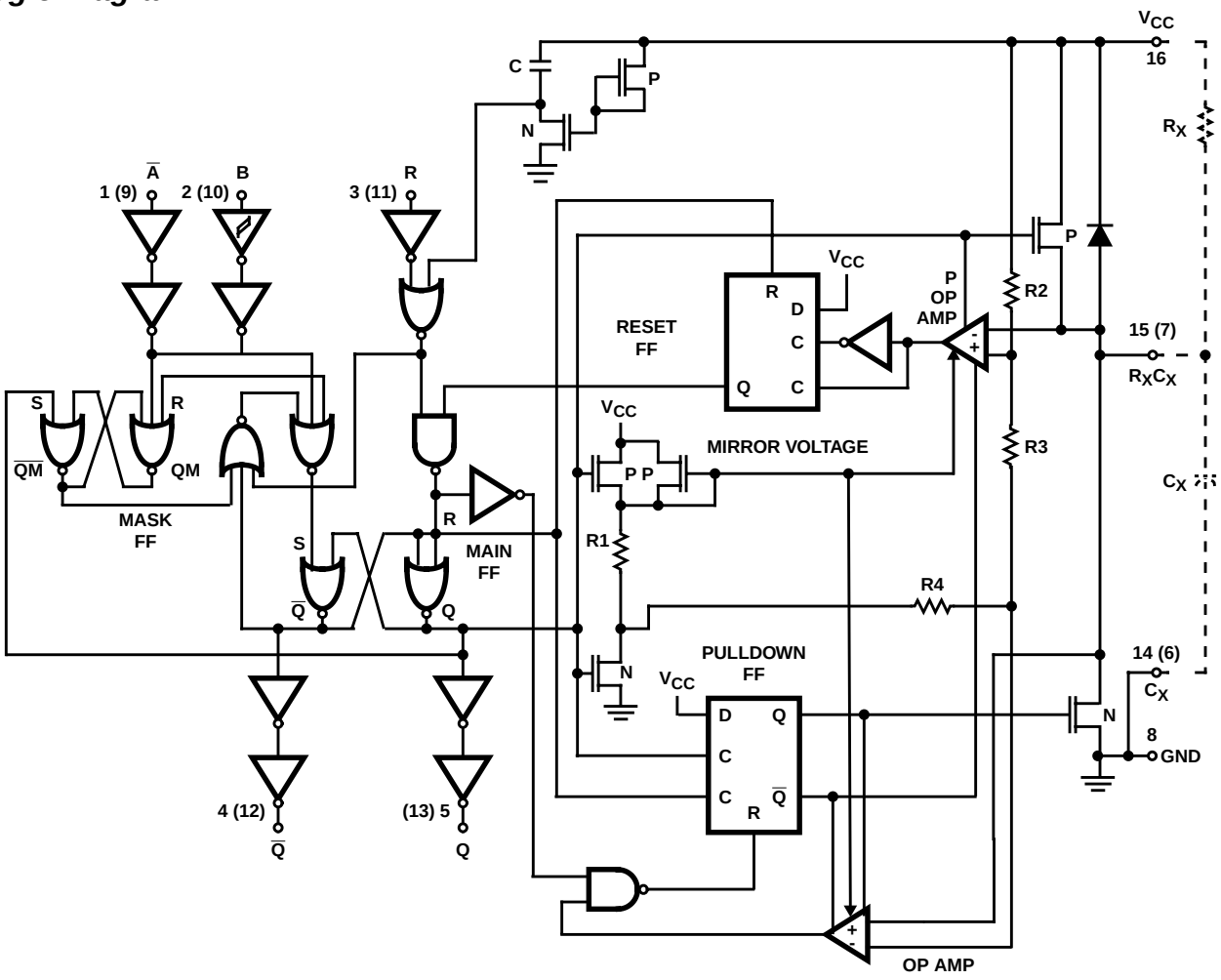
INPUTS			OUTPUTS	
$\overline{A}$	B	$\overline{R}$	Q	$\overline{Q}$
H	X	H	L	H
X	L	H	L	H
L	↑	H	⊓	⊔
↓	H	H	⊓	⊔
X	X	L	L	H
L	H	↑	⊓ (Note 3)	⊔ (Note 3)

H = High Voltage Level, L = Low Voltage Level, X = Irrelevant, ↑ = Transition from Low to High Level, ↓ = Transition from High to Low Level, ⊓ = One High Level Pulse, ⊔ = One Low Level Pulse

NOTE:

1. For this combination the reset input must be low and the following sequence must be used: pin 1 (or 9) must be set high or pin 2 (or 10) set low; then pin 1 (or 9) must be low and pin 2 (or 10) set high. Now the reset input goes from low-to-high and the device will be triggered.

Logic Diagram



Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Drain Current, per Output, I_O
For -0.5V < V_O < V_{CC} + 0.5V . . . . . ±25mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time, t_r, t_f on Inputs $\overline{A}$ and $\overline{R}$
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)
Input Rise and Fall Time, t_r, t_f on Input B
2V . . . . . Unlimited ns (Max)
4.5V. . . . . Unlimited ns (Max)
6V . . . . . Unlimited ns (Max)

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 2):
E (PDIP) Package . . . . . 67°C/W
M (SOIC) Package. . . . . 73°C/W
NS (SOP) Package . . . . . 64°C/W
PW (TSSOP) Package . . . . . 108°C/W
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	0	5.5	-		±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 3)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

3. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
All Inputs	0.3

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Prerequisite For Switching Function

PARAMETER	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
Input Pulse Width $\overline{A}$	t_{WL}	2	70	-	-	90	-	105	-	ns
		4.5	14	-	-	18	-	21	-	ns
		6	12	-	-	15	-	18	-	ns
Input Pulse Width B	t_{WH}	2	70	-	-	90	-	105	-	ns
		4.5	14	-	-	18	-	21	-	ns
		6	12	-	-	15	-	18	-	ns

Prerequisite For Switching Function (Continued)

PARAMETER	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Pulse Width Reset	t_{WL}	2	70	-	-	90	-	105	-	ns
		4.5	14	-	-	18	-	21	-	ns
		6	12	-	-	15	-	18	-	ns
Recovery Time $\overline{R}$ to $\overline{A}$ or B	t_{SU}	2	0	-	-	0	-	0	-	ns
		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
Output Pulse Width Q or $\overline{Q}$ C_X = 0.1µF R_X = 10kΩ	t_W	5	630	-	770	602	798	595	805	µs
Output Pulse Width Q or Q C_X = 28pF, R_X = 2kΩ	t_W	4.5	-	140	-	-	-	-	-	ns
C_X = 1000pF, R_X = 2kΩ	t_W	4.5	-	1.5	-	-	-	-	-	µs
C_X = 1000pF, R_X = 10kΩ	t_W	4.5	-	7	-	-	-	-	-	µs
HCT TYPES										
Input Pulse Width $\overline{A}$	t_{WL}	4.5	14	-	-	18	-	21	-	ns
Input Pulse Width B	t_{WH}	4.5	14	-	-	18	-	21	-	ns
Input Pulse Width Reset	t_{WL}	4.5	18	-	-	23	-	27	-	ns
Recovery Time $\overline{R}$ to $\overline{A}$ or B	t_{SU}	4.5	0	-	-	0	-	0	-	ns
Output Pulse Width Q or $\overline{Q}$ C_X = 0.1µF R_X = 10kΩ	t_W	5	630	-	770	602	798	595	805	µs
Output Pulse Width Q or Q C_X = 28pF, R_X = 2kΩ	t_W	4.5	-	140	-	-	-	-	-	ns
C_X = 1000pF, R_X = 2kΩ	t_W	4.5	-	1.5	-	-	-	-	-	µs
C_X = 1000pF, R_X = 10kΩ	t_W	4.5	-	7	-	-	-	-	-	µs

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay, Trigger $\overline{A}$, B, $\overline{R}$ to Q	t_{PLH}	C_L = 50pF	2	-	-	210	-	265	-	315	ns
		C_L = 50pF	4.5	-	-	42	-	53	-	63	ns
		C_L = 50pF	6	-	-	36	-	45	-	54	ns
		C_L = 15pF	5	-	18	-	-	-	-	-	ns
Propagation Delay, Trigger $\overline{A}$, B, $\overline{R}$ to $\overline{Q}$	t_{PHL}	C_L = 50pF	2	-	-	170	-	215	-	255	ns
		C_L = 50pF	4.5	-	-	34	-	43	-	51	ns
		C_L = 50pF	6	-	-	29	-	37	-	43	ns
		C_L = 15pF	5	-	14	-	-	-	-	-	ns

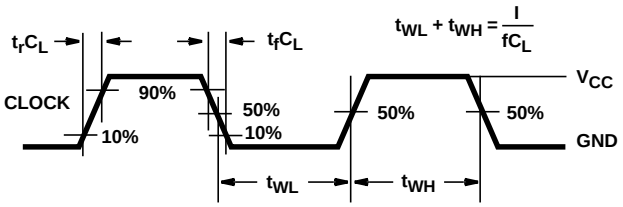
Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Propagation Delay, $\overline{R}$ to Q	t_{PLH}	C_L = 50pF	2	-	-	160	-	200	-	240	ns
			4.5	-	-	32	-	40	-	48	ns
			6	-	-	27	-	34	-	41	ns
Propagation Delay, $\overline{R}$ to $\overline{Q}$	t_{PHL}	C_L = 50pF	2	-	-	180	-	225	-	270	ns
			4.5	-	-	36	-	45	-	54	ns
			6	-	-	31	-	38	-	46	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_{IN}	-	-	-	-	10	-	10	-	10	pF
Pulse Width Match Between Circuits in the Same Package C_X = 1000pF, R_X = 10kΩ		-	4.5 to 5.5	-	±2	-	-	-	-	-	%
Power Dissipation Capacitance (Notes 4, 5)	CPD	-	5	-	166	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay, Trigger $\overline{A}$, B, $\overline{R}$ to Q	t_{PLH}	C_L = 50pF	4.5	-	-	42	-	-	-	63	ns
		C_L = 15pF	5	-	18	-	-	-	-	-	ns
Propagation Delay, Trigger $\overline{A}$, B, $\overline{R}$ to $\overline{Q}$	t_{PHL}	C_L = 50pF	4.5	-	-	34	-	43	-	51	ns
		C_L = 15pF	5	-	14	-	-	-	-	-	ns
Propagation Delay, $\overline{R}$ to Q	t_{PLH}	C_L = 50pF	4.5	-	-	38	-	-	-	57	ns
Propagation Delay, $\overline{R}$ to $\overline{Q}$	t_{PHL}	C_L = 50pF	4.5	-	-	37	-	-	-	56	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_{IN}	-	-	-	-	10	-	10	-	10	pF
Pulse Width Match Between Circuits in the Same Package C_X = 1000pF, R_X = 10kΩ		-	4.5 to 5.5	-	±2	-	-	-	-	-	%
Power Dissipation Capacitance (Notes 4, 5)	CPD	-	5	-	166	-	-	-	-	-	pF

NOTES:

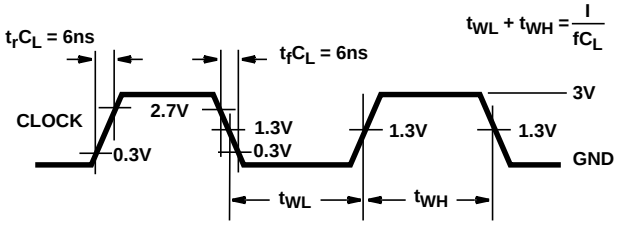
4. C_{PD} is used to determine the dynamic power consumption, per multivibrator.
5. $P_D = (C_{PD} + C_L) V_{CC}^2 f_i + \Sigma$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

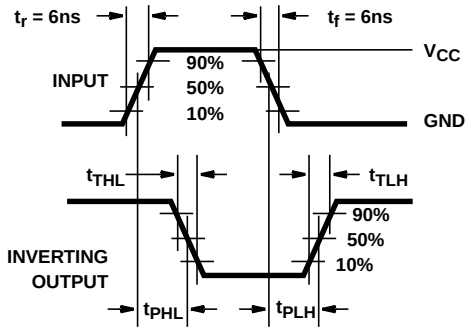


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

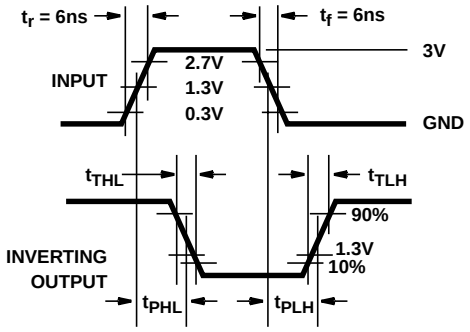


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

Typical Performance Curves

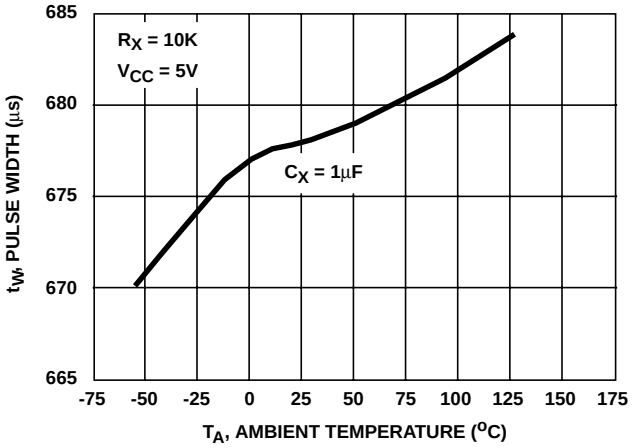


FIGURE 5. HC/HCT221 OUTPUT PULSE WIDTH vs TEMPERATURE

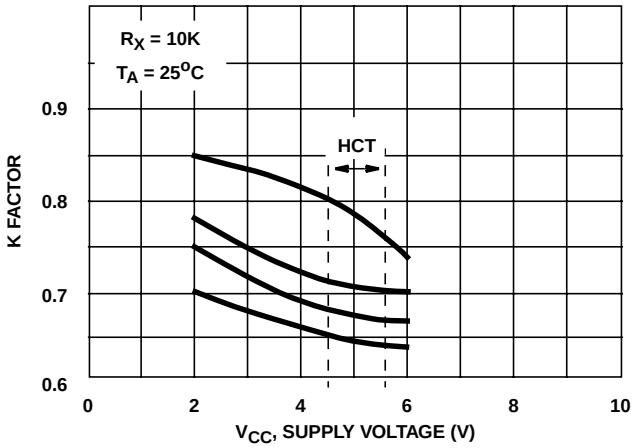


FIGURE 6. HC/HCT221 K FACTOR vs SUPPLY VOLTAGE

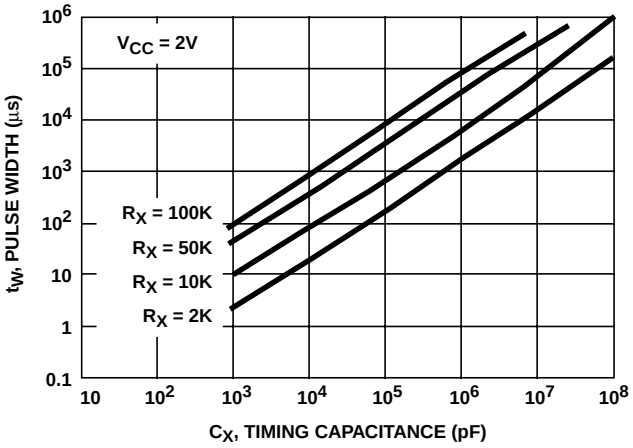


FIGURE 7. HC221 OUTPUT PULSE WIDTH vs C_X

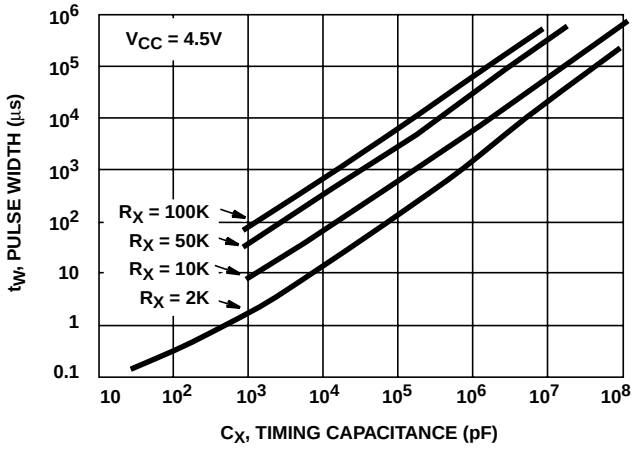


FIGURE 8. HC/HCT221 OUTPUT PULSE WIDTH vs C_X

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8780501EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8780501EA CD54HC221F3A	Samples
CD54HC221F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC221F	Samples
CD54HC221F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8780501EA CD54HC221F3A	Samples
CD74HC221E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC221E	Samples
CD74HC221EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC221E	Samples
CD74HC221M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC221M	Samples
CD74HC221M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC221M	Samples
CD74HC221M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC221M	Samples
CD74HC221MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC221M	Samples
CD74HC221MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC221M	Samples
CD74HC221NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC221M	Samples
CD74HC221PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ221	Samples
CD74HC221PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ221	Samples
CD74HC221PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ221	Samples
CD74HC221PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ221	Samples
CD74HC221PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ221	Samples
CD74HC221PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ221	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT221E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT221E	Samples
CD74HCT221EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT221E	Samples
CD74HCT221M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT221M	Samples
CD74HCT221M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT221M	Samples
CD74HCT221M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT221M	Samples
CD74HCT221M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT221M	Samples
CD74HCT221MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT221M	Samples
CD74HCT221MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT221M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD54HC221, CD74HC221 :

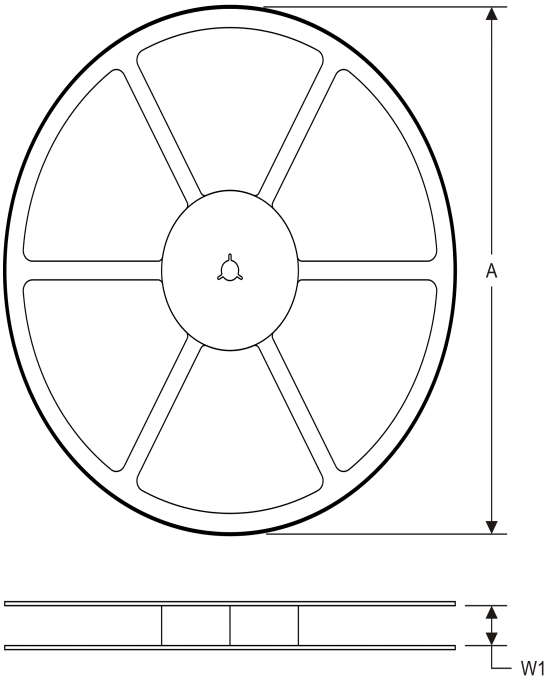
- Catalog: CD74HC221
- Military: CD54HC221

NOTE: Qualified Version Definitions:

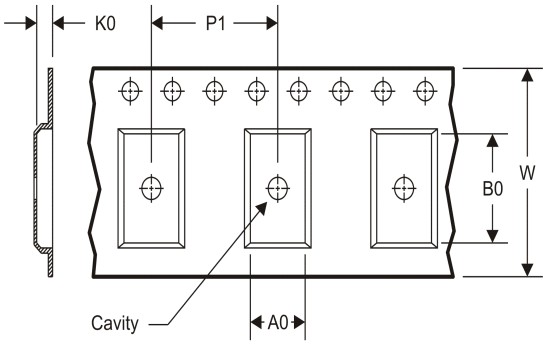
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



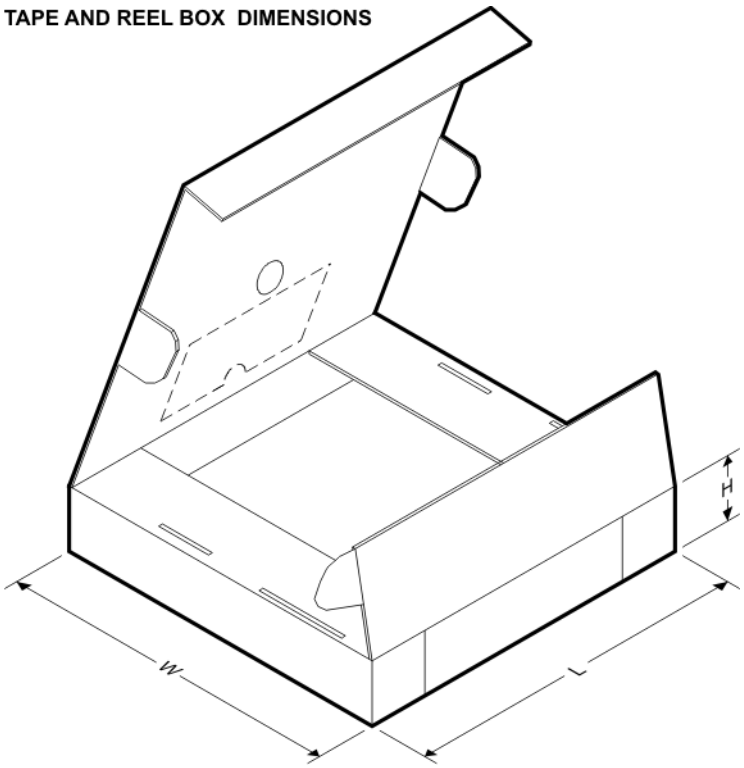
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC221M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC221NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC221PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC221PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT221M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

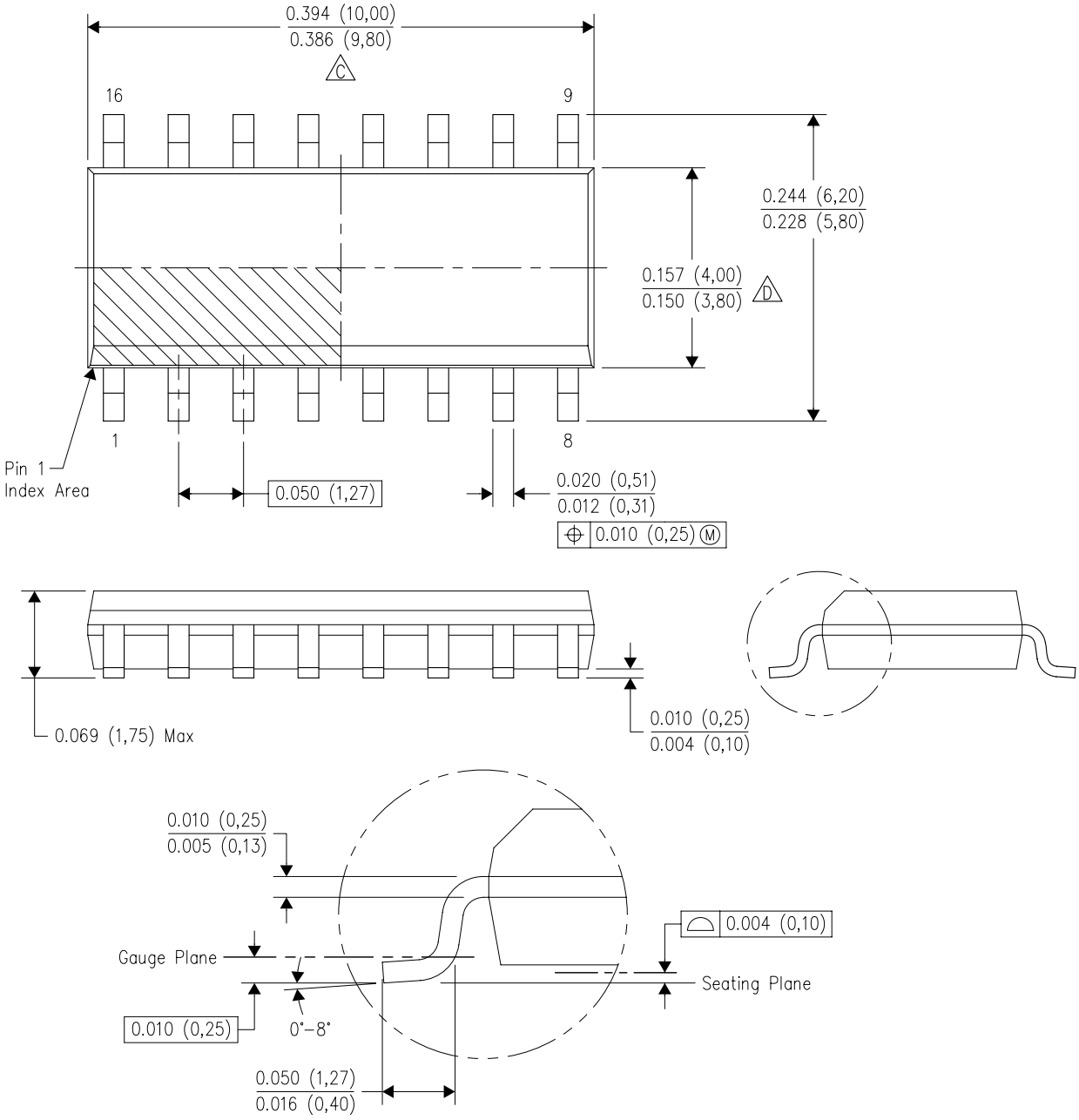
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

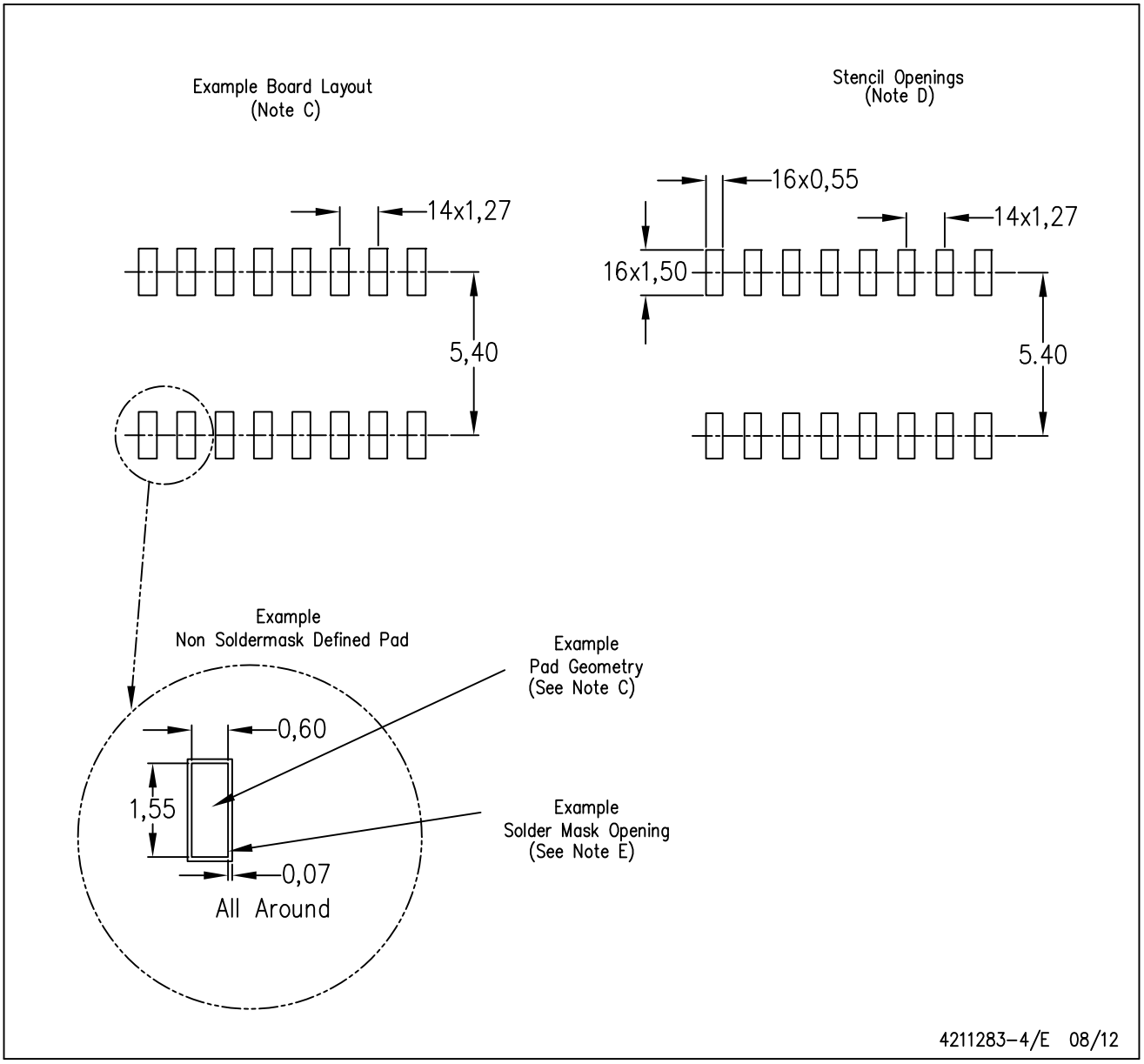
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC221M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC221NSR	SO	NS	16	2000	367.0	367.0	38.0
CD74HC221PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC221PWT	TSSOP	PW	16	250	367.0	367.0	35.0
CD74HCT221M96	SOIC	D	16	2500	333.2	345.9	28.6

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

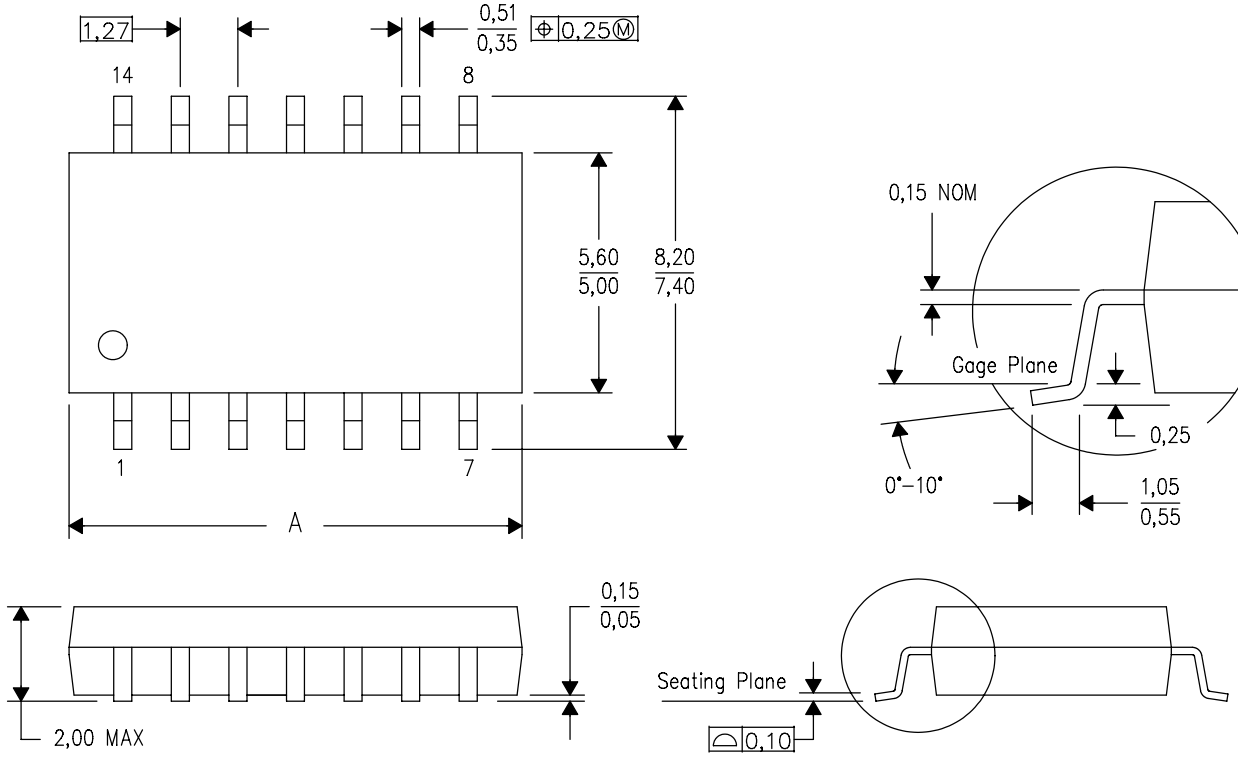


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

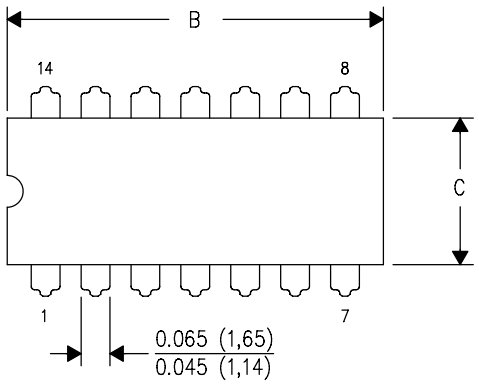
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

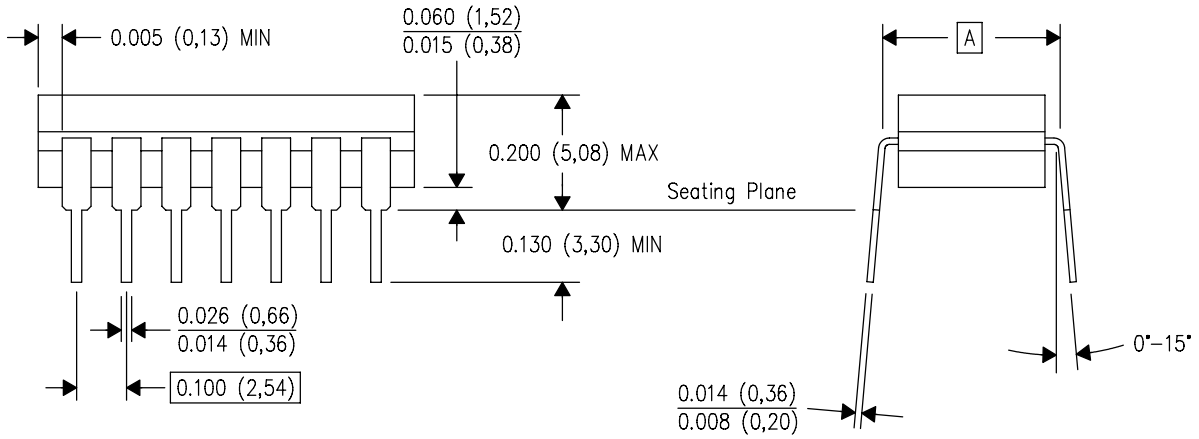
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



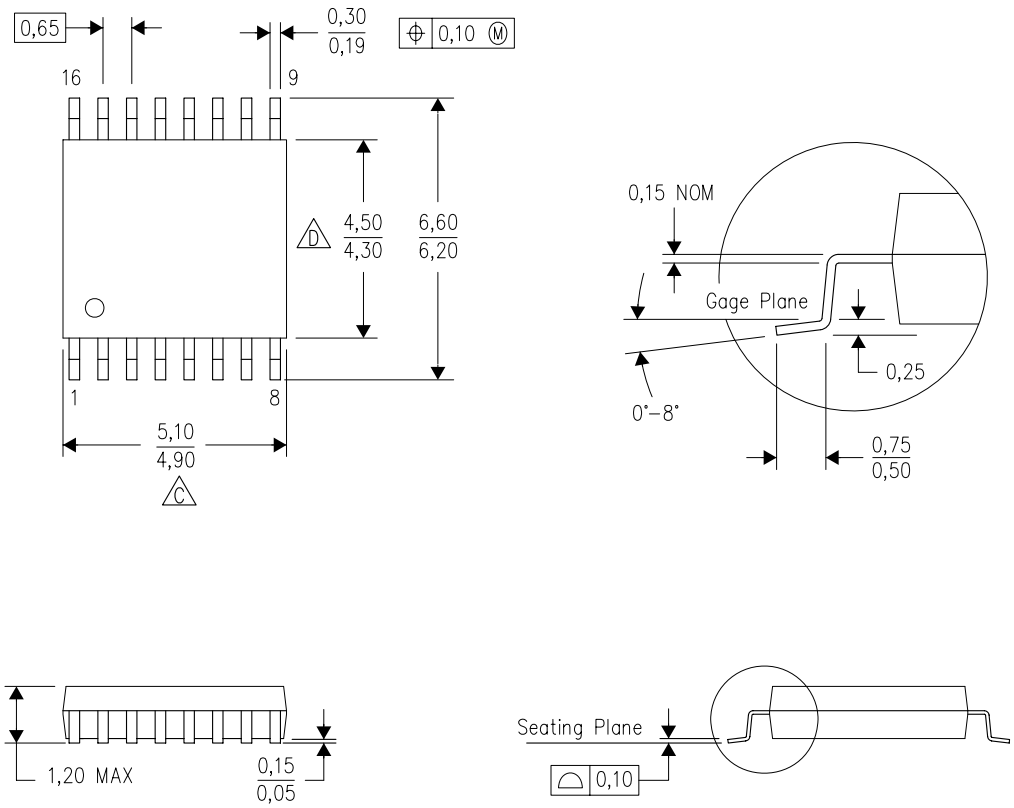
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

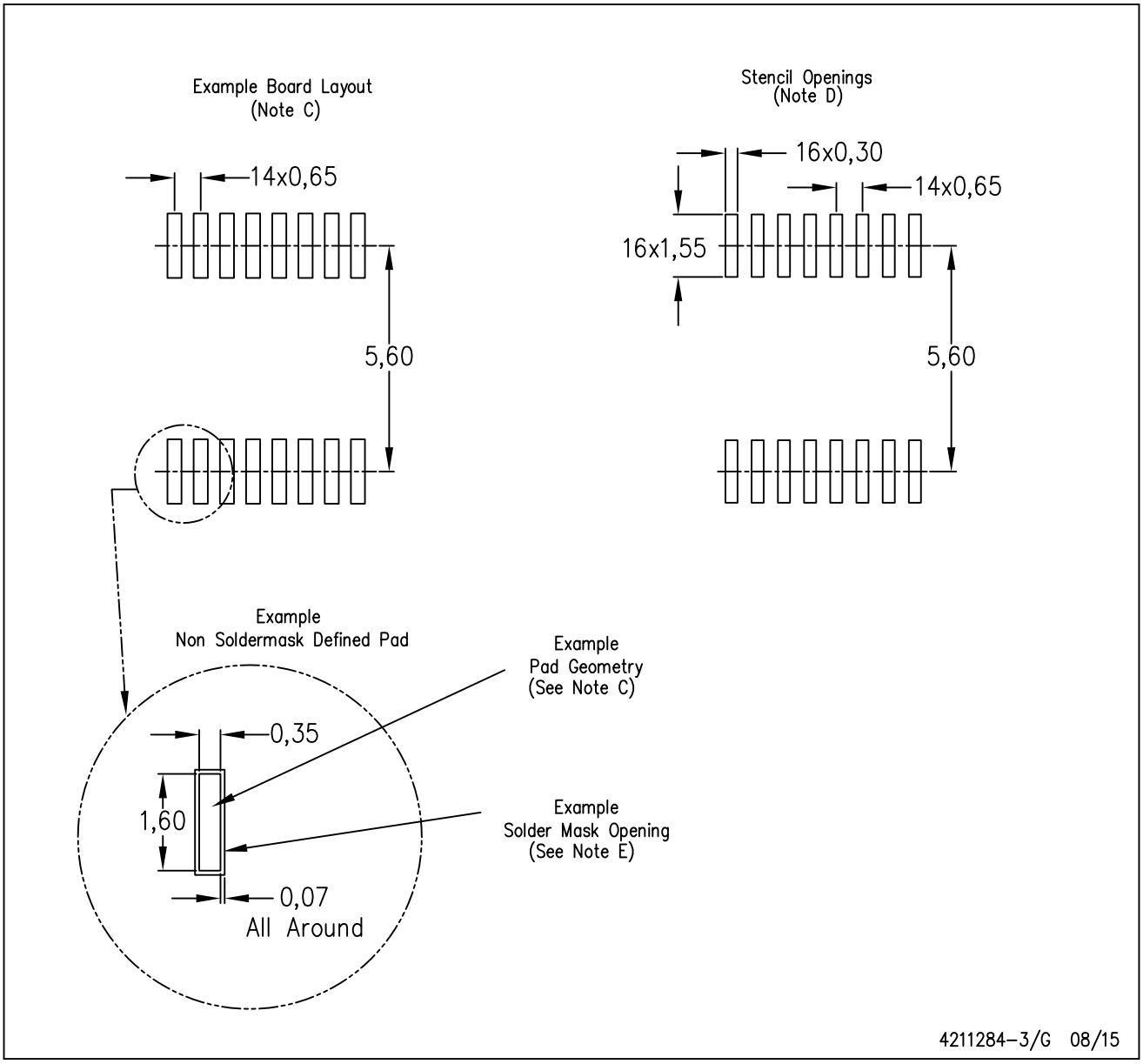
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE

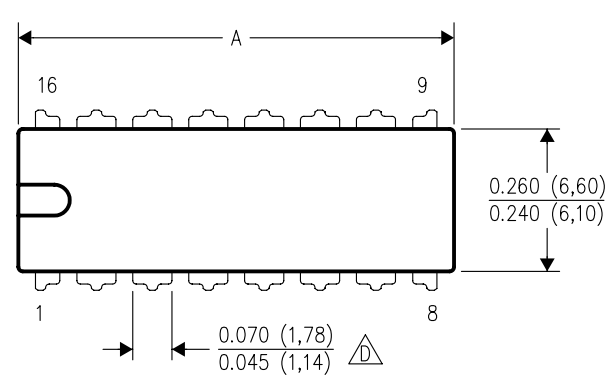


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

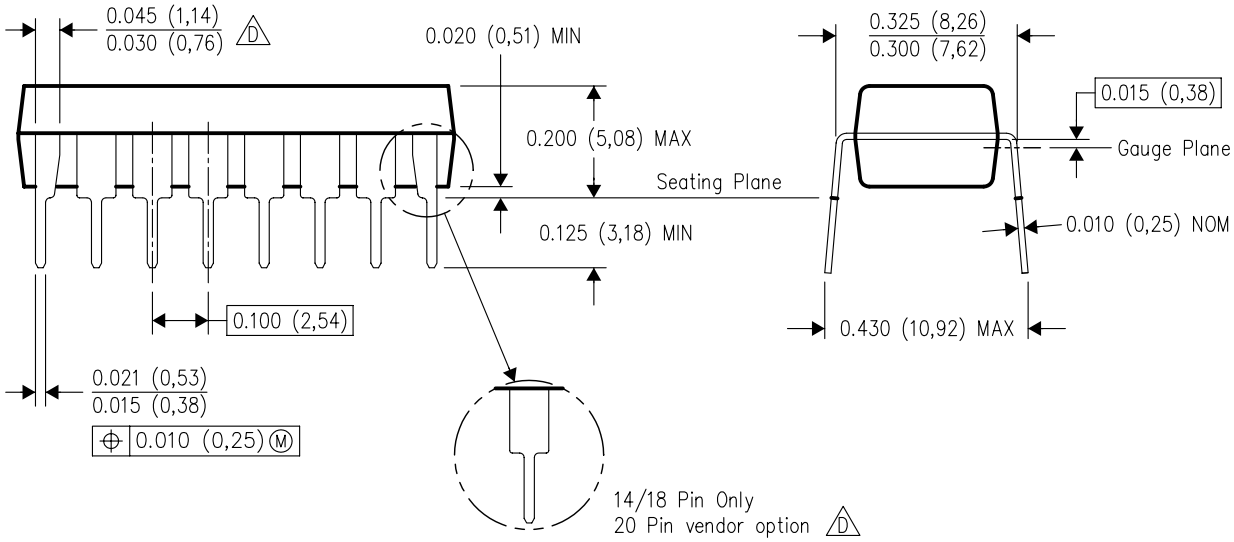
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265