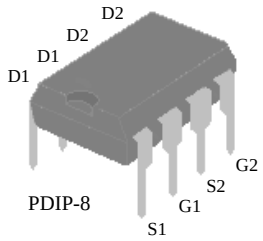
AP4511GD

RoHS-compliant Product

Advanced Power Electronics Corp.

N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

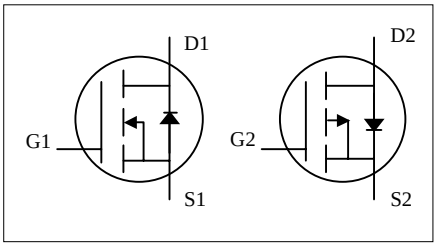
- **Low Gate Charge**
- **Fast Switching Speed**
- **PDIP-8 Package**



N-CH	BV_{DSS}	35V
	$R_{DS(ON)}$	25mΩ
	I_D	7A
P-CH	BV_{DSS}	-35V
	$R_{DS(ON)}$	40mΩ
	I_D	-6.1A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, ultra low on-resistance and cost-effectiveness.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	35	-35	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_A=25℃	Continuous Drain Current[3]	7	-6.1	A
I_D@T_A=70℃	Continuous Drain Current[3]	5.7	-5	A
I_{DM}	Pulsed Drain Current[1]	30	-30	A
P_D@T_A=25℃	Total Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/℃
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	62.5	℃/W

N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	35	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25℃, I_D=1mA	-	0.02	-	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=7A	-	20	25	mΩ
		V_{GS}=4.5V, I_D=5A	-	30	37	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	-	3	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=7A	-	9	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=35V, V_{GS}=0V	-	-	1	uA
	Drain-Source Leakage Current (T_j=70°C)	V_{DS}=28V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=7A	-	11	18	nC
Q_{gs}	Gate-Source Charge	V_{DS}=28V	-	3	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=4.5V	-	6	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=18V	-	12	-	ns
t_r	Rise Time	I_D=1A	-	7	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω,V_{GS}=10V	-	22	-	ns
t_f	Fall Time	R_D=18Ω	-	6	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	830	1330	pF
C_{oss}	Output Capacitance	V_{DS}=25V	-	150	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	110	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1.2	1.8	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=1.7A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time[2]	I_S=7A, V_{GS}=0V	-	18	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	12	-	nC

P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-35	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25℃,I_D=-1mA	-	-0.02	-	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V, I_D=-6A	-	35	40	mΩ
		V_{GS}=-4.5V, I_D=-4A	-	53	60	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1	-	-3	V
g_{fs}	Forward Transconductance	V_{DS}=-10V, I_D=-6A	-	9	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-35V, V_{GS}=0V	-	-	-1	uA
	Drain-Source Leakage Current (Tj=70°C)	V_{DS}=-28V, V_{GS}=0V	-	-	-25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=-6A	-	10	16	nC
Q_{gs}	Gate-Source Charge	V_{DS}=-28V	-	2	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=-4.5V	-	6	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=-18V	-	10	-	ns
t_r	Rise Time	I_D=-1A	-	6	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω,V_{GS}=-10V	-	26	-	ns
t_f	Fall Time	R_D=18Ω	-	7	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	690	1100	pF
C_{oss}	Output Capacitance	V_{DS}=-25V	-	165	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	130	-	pF
R_g	Gate Resistance	f=1.0MHz	-	5.2	7.8	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=-1.7A, V_{GS}=0V	-	-	-1.2	V
t_{rr}	Reverse Recovery Time[2]	I_S=-6A, V_{GS}=0V	-	20	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=-100A/μs	-	12	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board , t ≤10sec ; 90℃/W when mounted on min. copper pad.

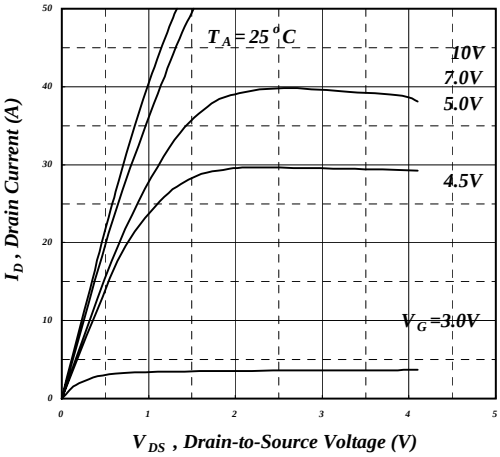


Fig 1. Typical Output Characteristics

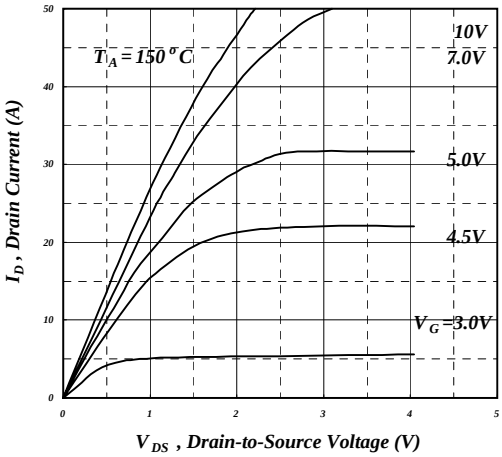


Fig 2. Typical Output Characteristics

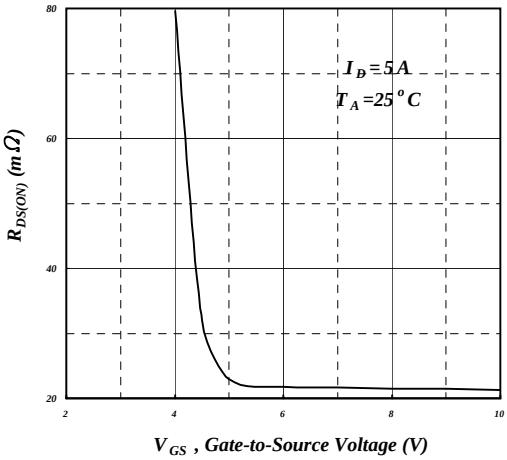


Fig 3. On-Resistance v.s. Gate Voltage

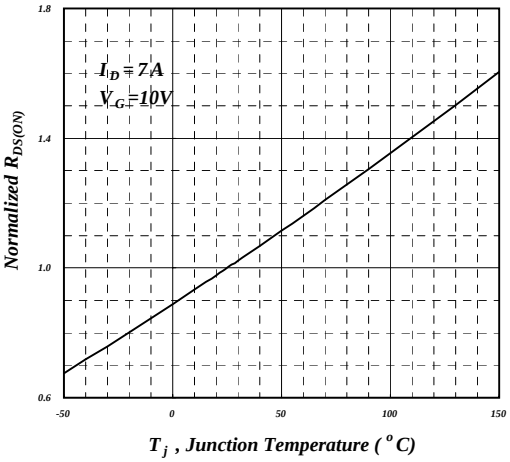


Fig 4. Normalized On-Resistance v.s. Junction Temperature

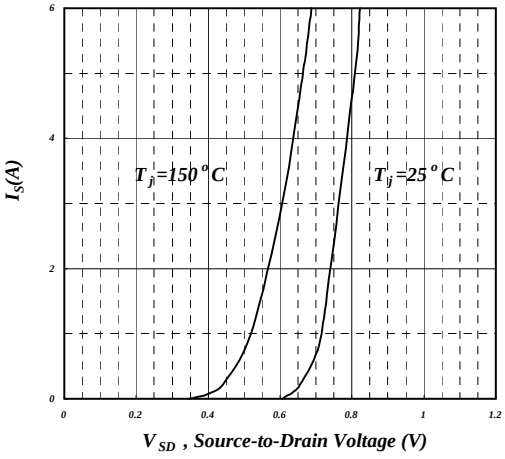


Fig 5. Forward Characteristic of Reverse Diode

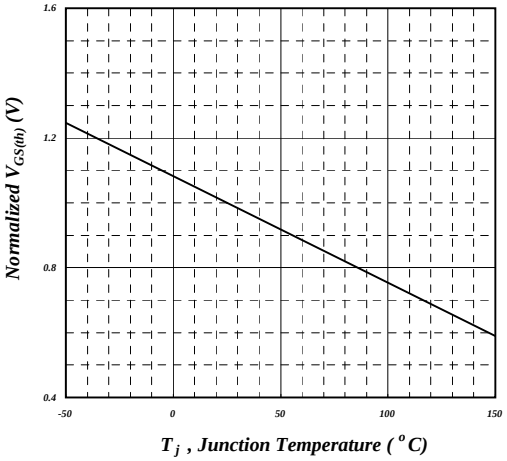


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

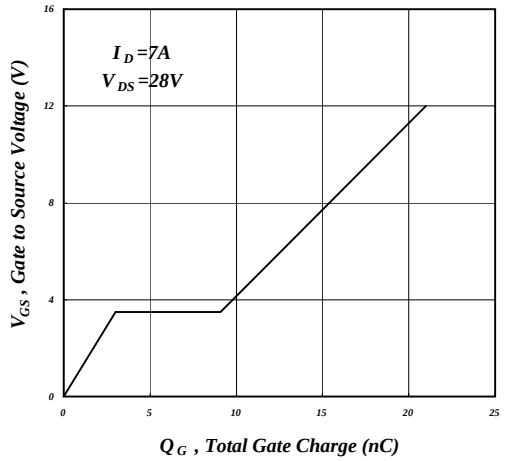


Fig 7. Gate Charge Characteristics

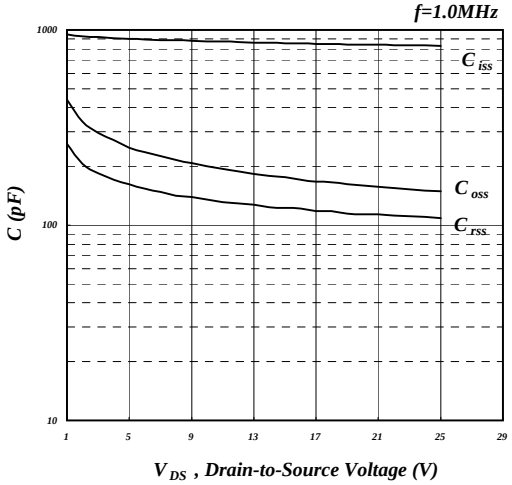


Fig 8. Typical Capacitance Characteristics

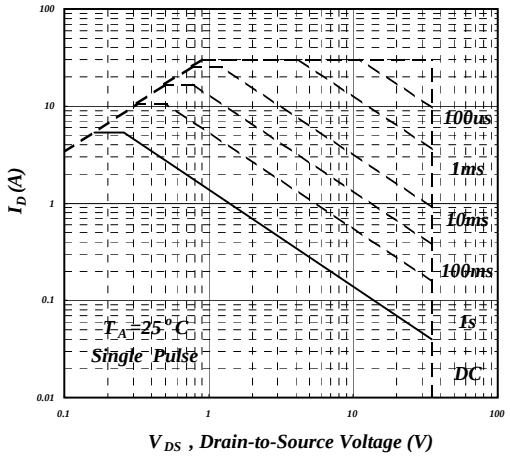


Fig 9. Maximum Safe Operating Area

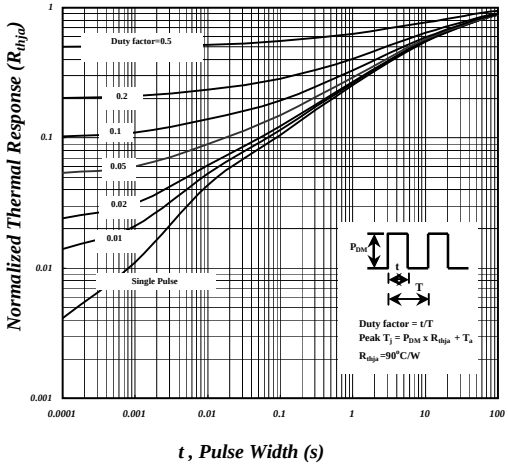


Fig 10. Effective Transient Thermal Impedance

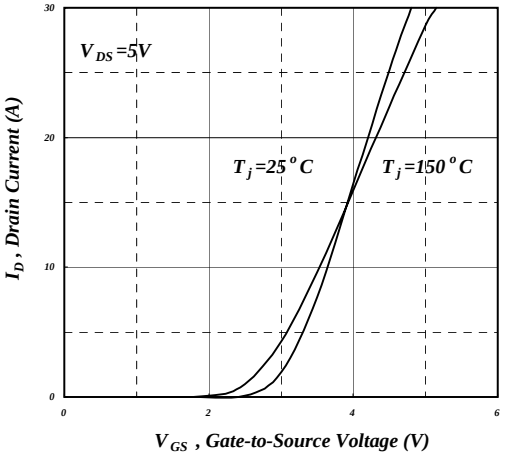


Fig 11. Transfer Characteristics

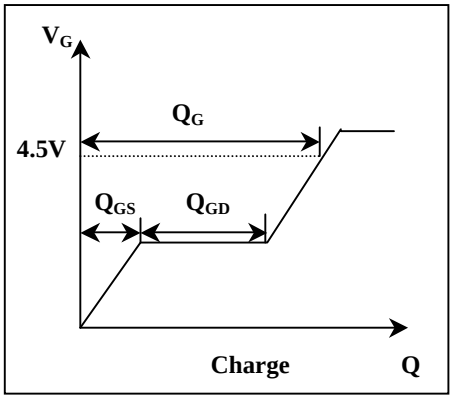


Fig 12. Gate Charge Waveform

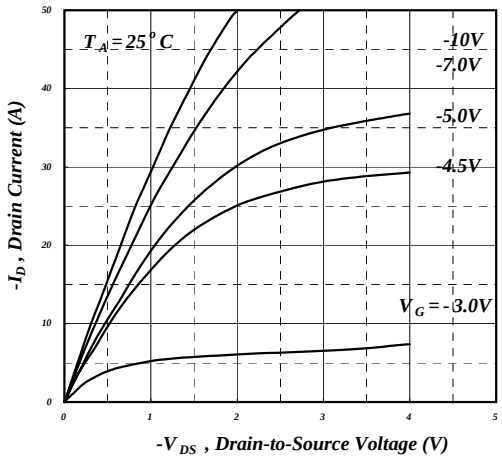


Fig 1. Typical Output Characteristics

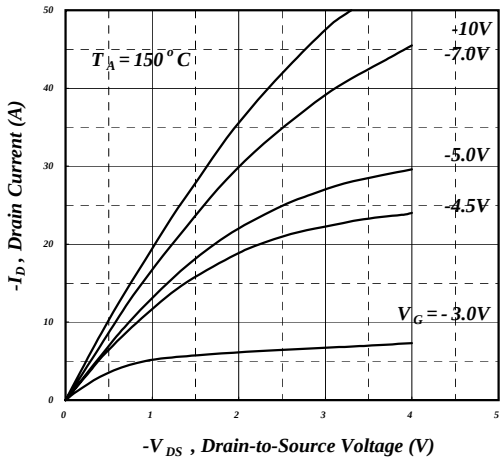


Fig 2. Typical Output Characteristics

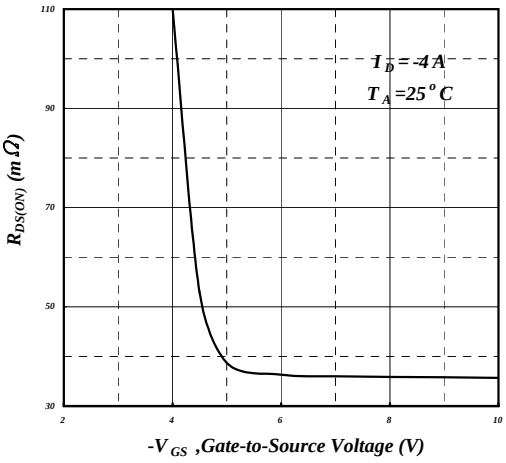


Fig 3. On-Resistance v.s. Gate Voltage

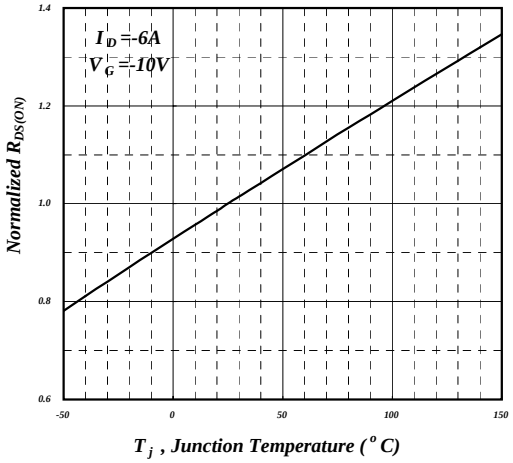


Fig 4. Normalized On-Resistance v.s. Junction Temperature

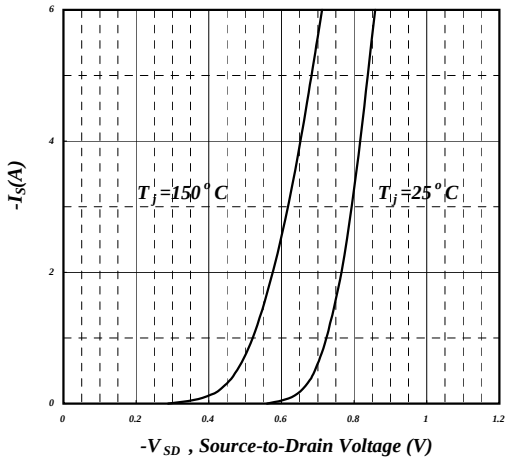


Fig 5. Forward Characteristic of Reverse Diode

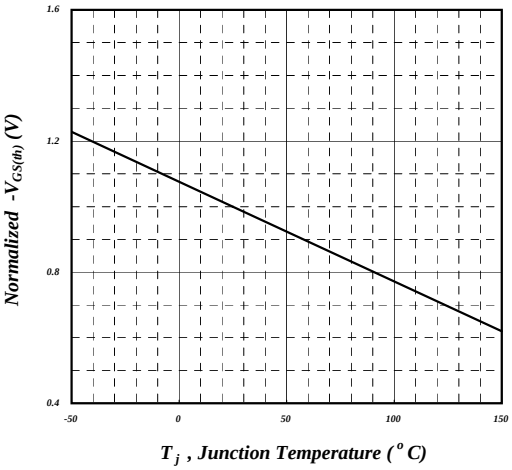


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

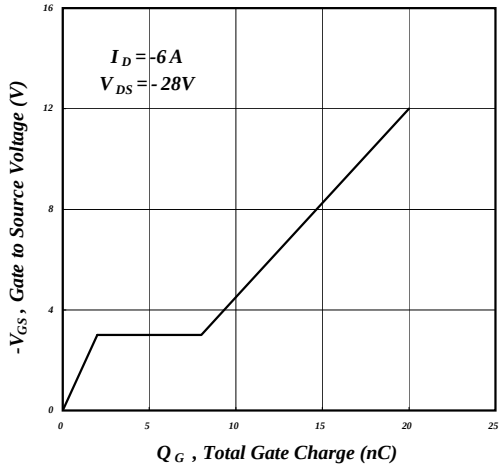


Fig 7. Gate Charge Characteristics

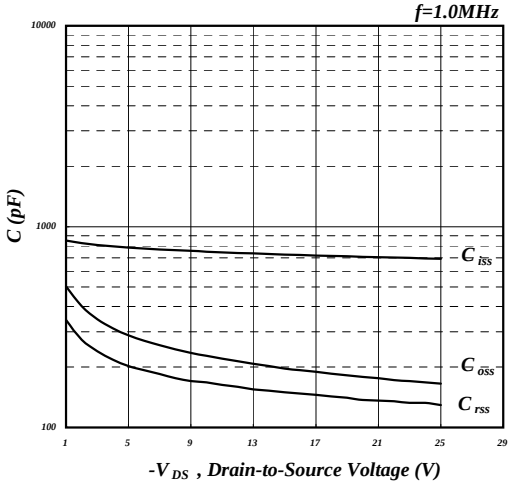


Fig 8. Typical Capacitance Characteristics

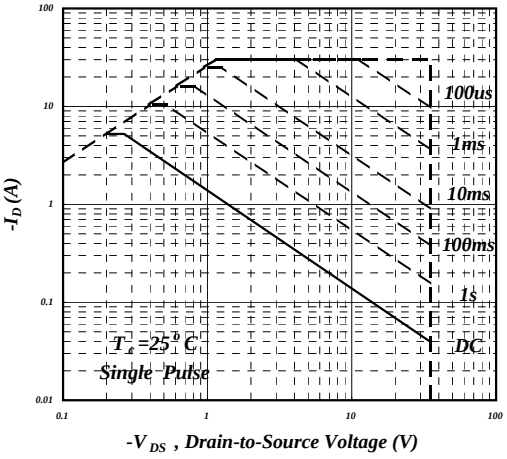


Fig 9. Maximum Safe Operating Area

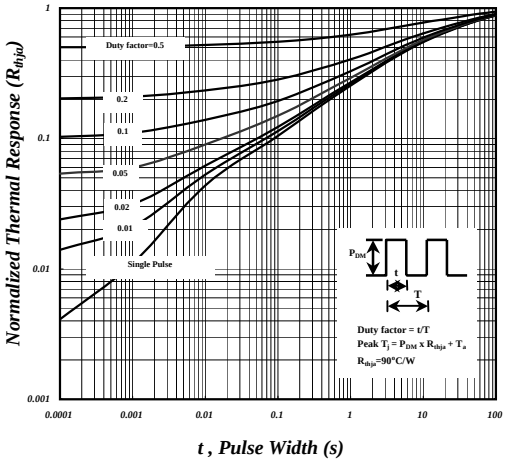


Fig 10. Effective Transient Thermal Impedance

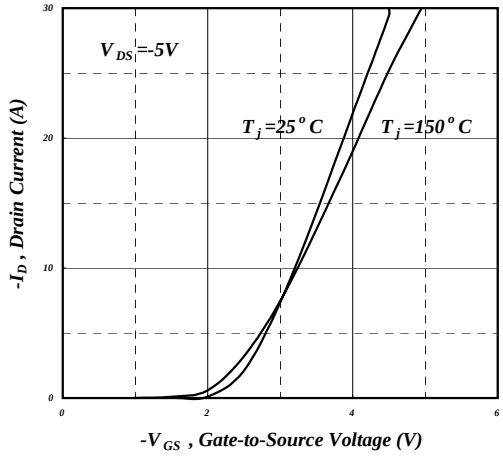


Fig 11. Transfer Characteristics

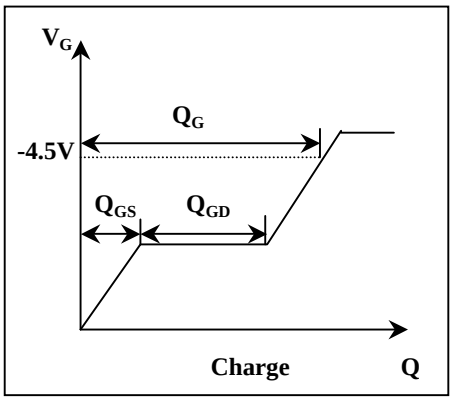
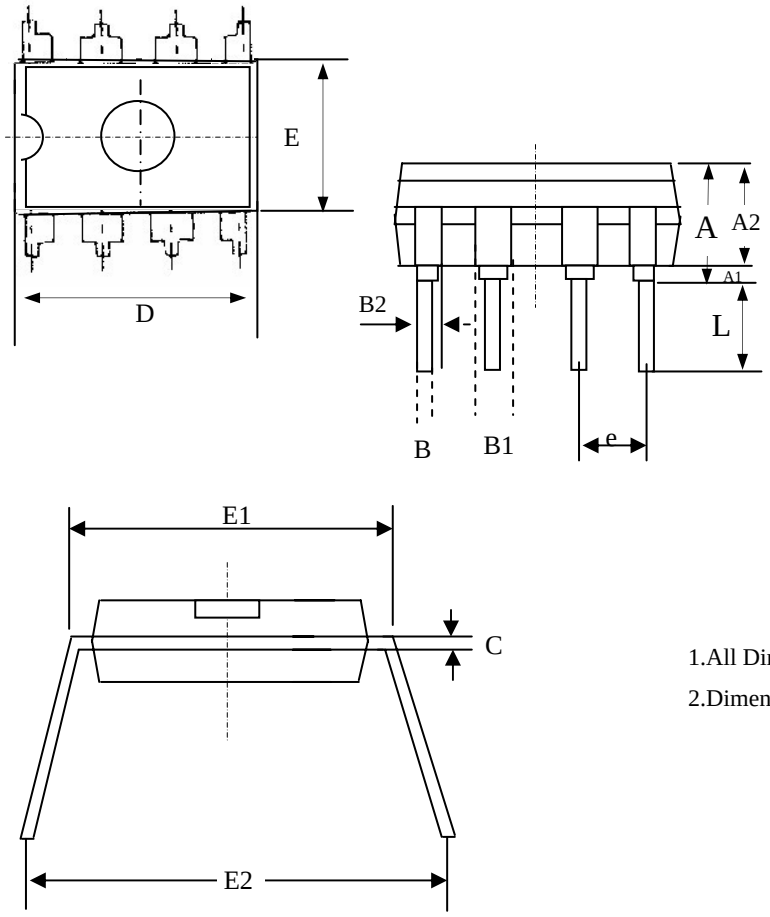


Fig 12. Gate Charge Waveform

Package Outline : DIP-8

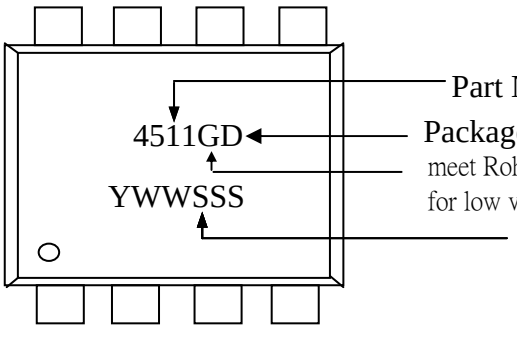


SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	3.60	4.50	5.40
A1	0.38	----	----
A2	2.90	3.95	5.00
B	0.36	0.46	0.56
B1	1.10	1.45	1.80
B2	0.76	0.98	1.20
C	0.20	0.28	0.36
D	9.00	9.60	10.20
E	6.10	6.65	7.20
E1	7.62	7.94	8.26
E2	8.30	9.65	11.00
e	2.540 BSC		
L	3.18	----	----

1.All Dimensions Are in Millimeters.

2.Dimension Does Not Include Mold Protrusions.

Part Marking Information & Packing : DIP-8



Part Number

Package Code

meet Rohs requirement

for low voltage MOSFET only

Date Code (YWWSSS)

Y：Last Digit Of The Year

WW：Week

SSS：Sequence