



# TDA7250

## 60 W HI-FI DUAL AUDIO DRIVER

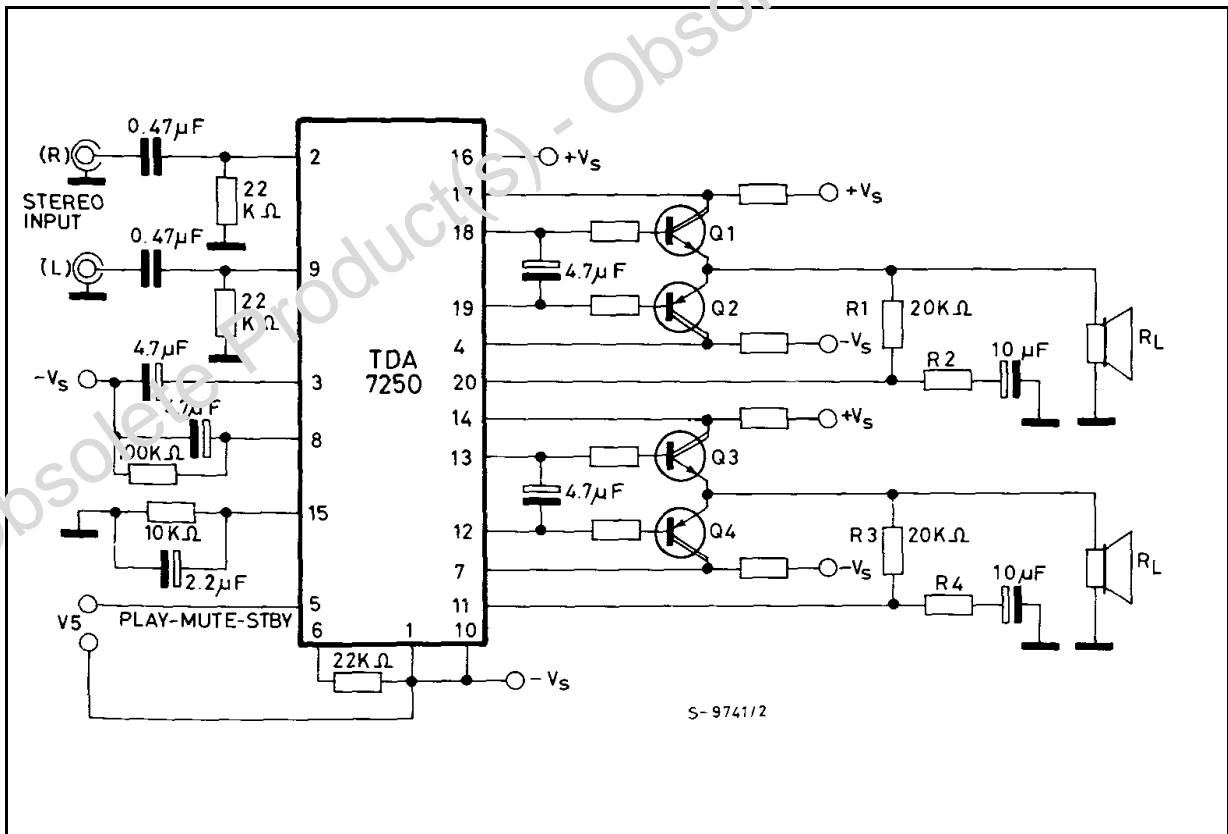
- WIDE SUPPLY VOLTAGE RANGE : 20 TO 90 V ( $\pm 10$  to  $\pm 45$  V)
- VERY LOW DISTORTION
- AUTOMATIC QUIESCENT CURRENT CONTROL FOR THE POWER TRANSISTORS WITHOUT TEMPERATURE SENSE ELEMENTS
- OVERLOAD CURRENT PROTECTION FOR THE POWER TRANSISTORS
- MUTE/STAND-BY FUNCTIONS
- LOW POWER CONSUMPTION
- OUTPUT POWER 60 W/8  $\Omega$  AND 100 W/4  $\Omega$

### DESCRIPTION

The TDA7250 stereo audio driver is designed to drive two pair of complementary output transistor in the Hi-Fi power amplifiers.

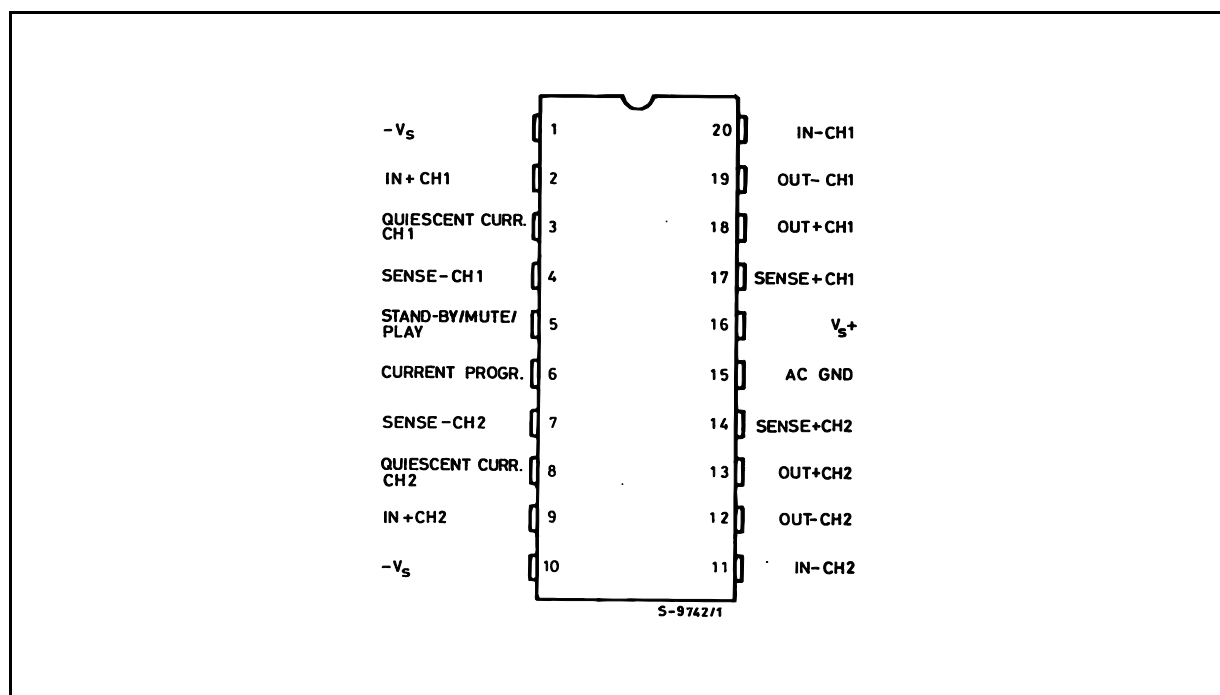


### APPLICATION CIRCUIT



## TDA7250

### PIN CONNECTION (top view)



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_s$	Supply Voltage	100	V
$P_{tot}$	Power Dissipation at $T_{amb} = 60\text{ }^\circ\text{C}$	1.4	W
$T_j, T_{stg}$	Storage and Junction Temperature	- 40 to + 150	$^\circ\text{C}$

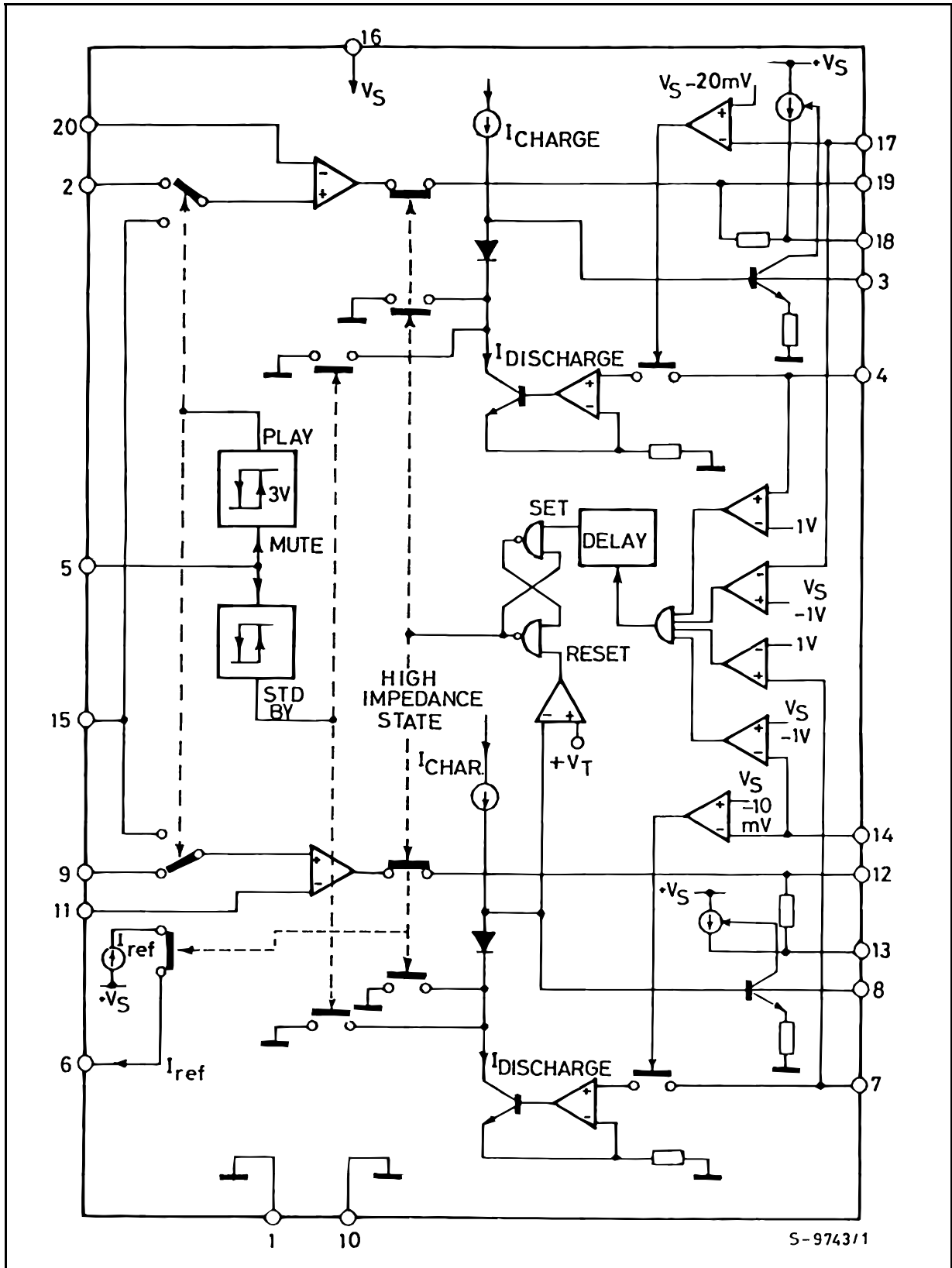
### THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max. 65	$^\circ\text{C/W}$

## PIN FUNCTIONS

N°	Name	Function
1	V <sub>S</sub> – POWER SUPPLY	Negative Supply Voltage.
2	NON-INV. INP. CH. 1	Channel 1 Input Signal.
3	QUIESC. CURRENT CONTR. CAP. CH1	This capacitor works as an integrator, to control the quiescent current to output devices in no-signal conditions on channel 1.
4	SENSE (-) CH. 1	Negative voltage sense input for overload protection and for automatic quiescent current control.
5	ST. BY / MUTE / PLAY	Three-functions Terminal. For V <sub>IN</sub> = 1 to 3 V, the device is in MUTE and only quiescent current flows in the power stages ; - for V <sub>IN</sub> < 1 V, the device is in STAND-BY mode and no quiescent current is present in the power stages ; - for V <sub>IN</sub> > 3 V, the device
6	CURRENT PROGRAM	High Impedance Power-stages Monitor.
7	SENSE (-) CH. 2	Negative Voltage Sense Input for Overload Protection and for Automatic Quiescent Current Control.
8	QUIESC. CURRENT CONTR. CAP. CH. 2	This capacitor works as an integrator, to control the quiescent current to output devices in no-signal conditions on channel 2. If the voltage at its terminals drops under 250 mV, it also resets the device from high-impedance state of output stages.
9	NON-INV. INP. CH. 2	Channel 2 Input Signals.
10	V <sub>S</sub> – POWER SUPPLY	Negative Supply Voltage.
11	INVERT. INP. CH. 2	Feedback from Output (channel 2).
12	OUT (-) CH. 2	Out Signal to Lower Driver Transistor of Channel 2.
13	OUT (+) CH. 2	Out Signal to Higher Driver Transistor of Channel 2.
14	SENSE (+) CH. 2	Positive Voltage Sense Input for Overload Protection and for Automatic Quiescent Current Control.
15	COMMON AC GROUND	AC Input Ground in MUTE Condition.
16	V <sub>S</sub> + POWER SUPPLY	Positive Supply Voltage.
17	SENSE (+) CH. 1	Positive Voltage Sense Input for Overload Protection and for Automatic Quiescent Current Control.
18	OUT (+) CH. 1	Out Signal to High Driver Transistor of Channel 1.
19	OUT (-) CH. 1	Out Signal to Low Driver Transistor of Channel 1.
20	INVERT. INP. CH. 1	Feedback from Output (channel 1).

BLOCK DIAGRAM



**ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ ,  $V_s = \pm 35\text{ V}$ , play mode, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_s$	Supply Voltage		$\pm 10$		$\pm 45$	V
$I_d$	Quiescent Drain Current	Stand-by Mode		8		mA
		Play Mode		10	14	
$I_b$	Input Bias Current			0.2	1	$\mu\text{A}$
$V_{os}$	Input Offset Voltage			1	$\pm 10$	mV
$I_{os}$	Input Offset Current			100	200	nA
$G_v$	Open Loop Voltage Gain	$f = 100\text{ Hz}$		90		dB
		$f = 10\text{ kHz}$		60		
$e_N$	Input Noise Voltage	$R_G = 600\ \Omega$ $B = 20\text{ Hz to } 20\text{ kHz}$		3		$\mu\text{V}$
SR	Slew Rate			10		V/ $\mu\text{s}$
d	Total Harmonic Distortion	$G_v = 26\text{ dB}$ , $P_o = 40\text{ W}$ $f = 1\text{ kHz}$ $f = 20\text{ kHz}$		0.004		%
				0.03		%
$V_{opp}$	Output Voltage Swing			60		$V_{pp}$
$P_o$	Output Power (*)	$V_s = \pm 35\text{ V}$ , $R_L = 8\ \Omega$ $V_s = \pm 30\text{ V}$ , $R_L = 8\ \Omega$ $V_s = \pm 35\text{ V}$ , $R_L = 4\ \Omega$		60		W
				40		W
				100		W
$I_o$	Output Current			$\pm 5$		mA
SVR	Supply Voltage Rejection	$f = 100\text{ Hz}$		75		dB
$C_s$	Channel Separation	$f = 1\text{ kHz}$		75		dB

#### MUTE / STANDBY/ PLAY FUNCTIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_i$	Input Current (pin 5)			0.1		$\mu\text{A}$
$V_{th}$	Comparator Standby / Mute Threshold (**)		1.0	1.25	1.5	V
H	Hysteresis Standby / Mute			200		mV
$V_{th}$	Comparator Mute / Play Threshold (**)		2.4	3.0	3.6	V
H	Hysteresis Mute / Play			300		mV
	Mute Attenuation	$f = 1\text{ kHz}$		60		dB
$V_i$	Input Voltage Max. (pin 5)		12 (**)			V

(\*) Application circuit of fig. 1  $f = 1\text{ KHz}$ ;  $d = 0.1\%$ ;  $G_v = 26\text{ dB}$ .

(\*\*) Referred to  $-V_s$ .

#### CURRENT SURVEY CIRCUITRY

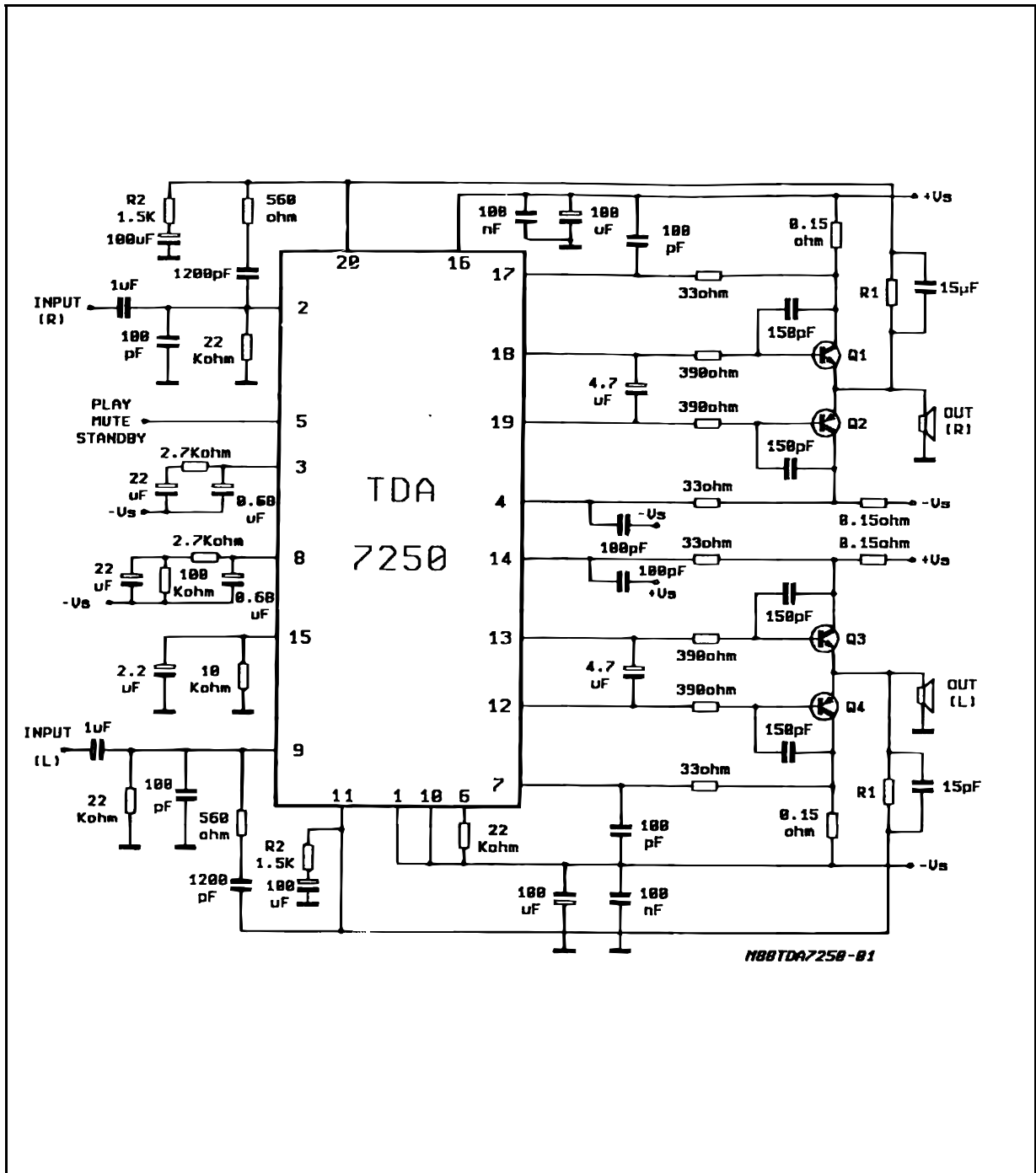
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Comparator Reference	to $+V_s$	0.8	1	1.4	V
		to $-V_s$	0.8	1	1.4	V
$t_d$	Delay Time		10			$\mu\text{s}$

#### QUIESCENT CURRENT CONTROL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Capacitor Current	Charge	30	60		$\mu\text{A}$
		Discharge	250	500		$\mu\text{A}$
	Comparator Reference	to $+V_s$	10	20	25	mV
		to $-V_s$		10		mV

# TDA7250

Figure 1 : Application Circuit with Power Darlings.



Note : Q1/Q2 = Q3/Q4 = TIP 142/TIP147  
 $GV = 1 + R1/R2$

Figure 2 : Output Power vs. Supply Voltage.

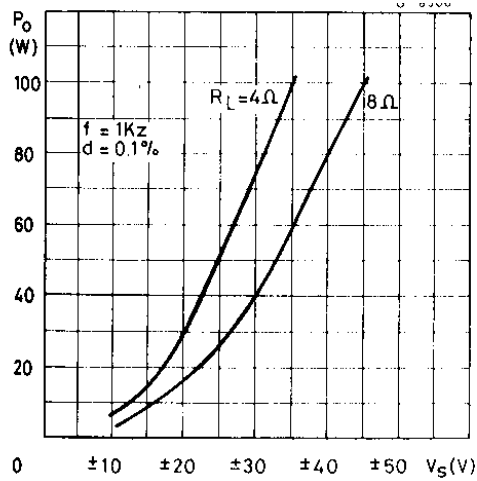


Figure 4 : Channel Separation.

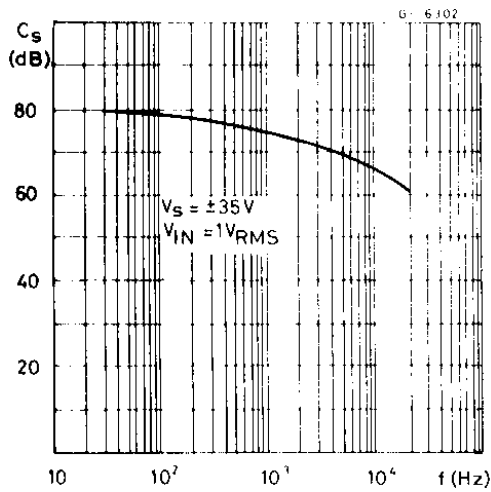


Figure 6 : Quiescent Current vs. Supply Voltage.

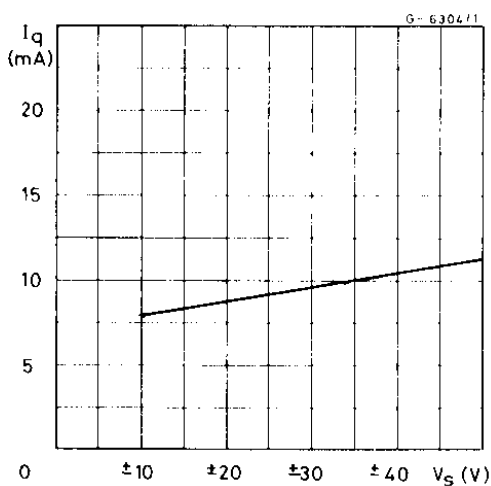


Figure 3 : Distortion vs. Output Power (\*).

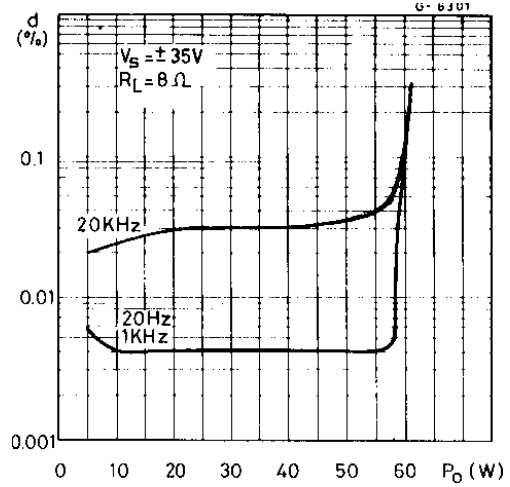


Figure 5 : Supply Voltage Rejection vs. Frequency.

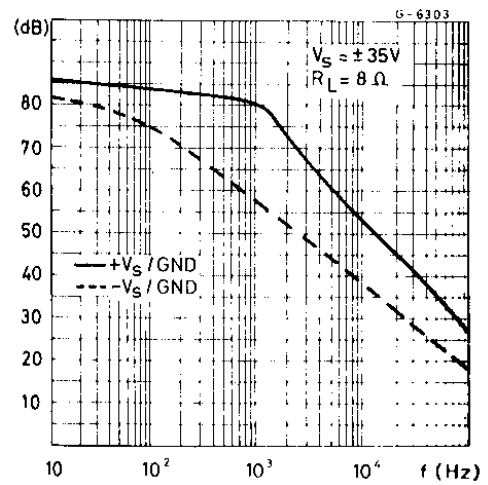


Figure 7 : Quiescent Current vs. T\_amb.

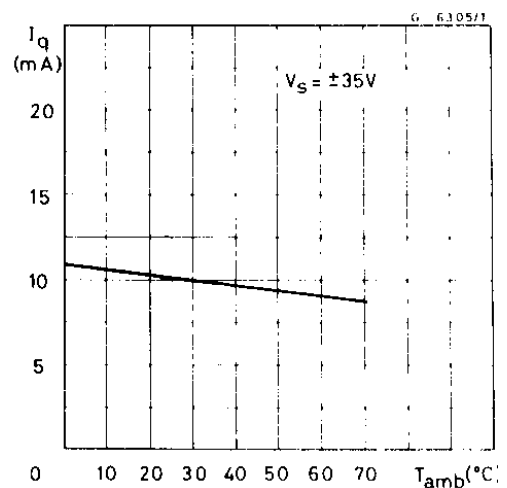


Figure 8 : Total Dissipated Power vs. Output Power (\*).

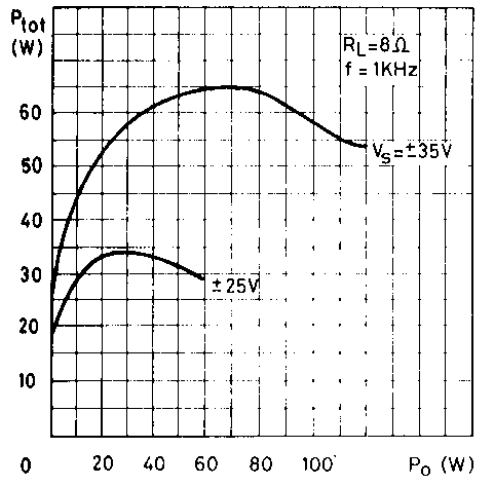


Figure 9 : Efficiency vs. Output Power (\*).

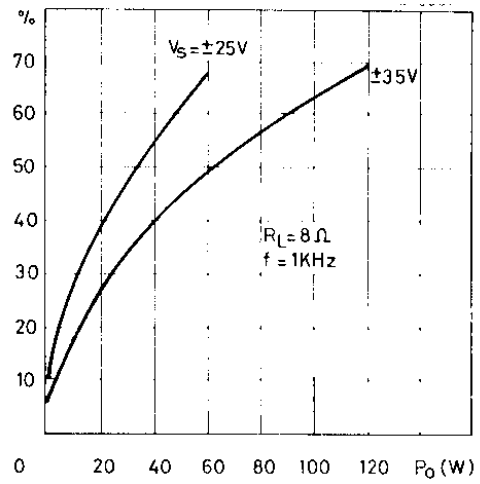
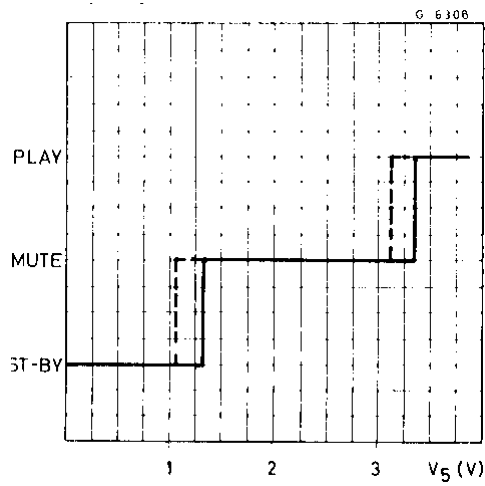


Figure 10 : Play-mute Standby Operation.



(\* Complete circuit



Figure 11 : Application Circuit Using Power Transistors.

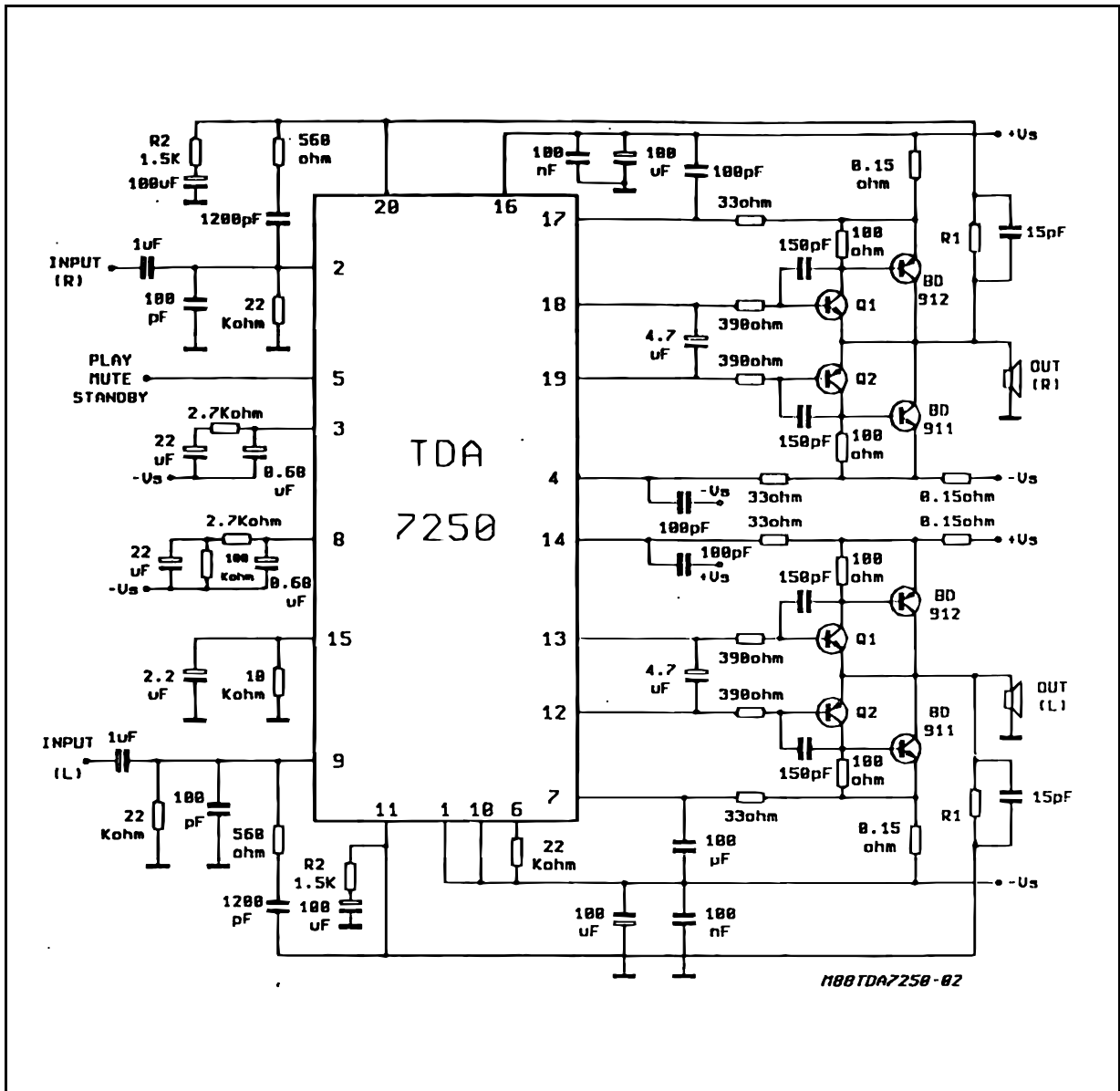


Figure 12 : Suggested Transistor Types for Various Loads and Powers.

$R_L = 8 \Omega$

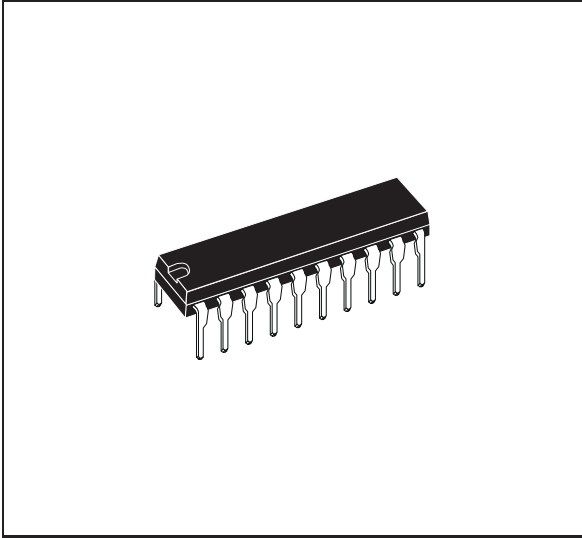
15W	+30W	+50W	+70W
BDX 53/54A	BDX 53/54B	BDW 93/94B	TIP 142/147

$T_L = 4 \Omega$

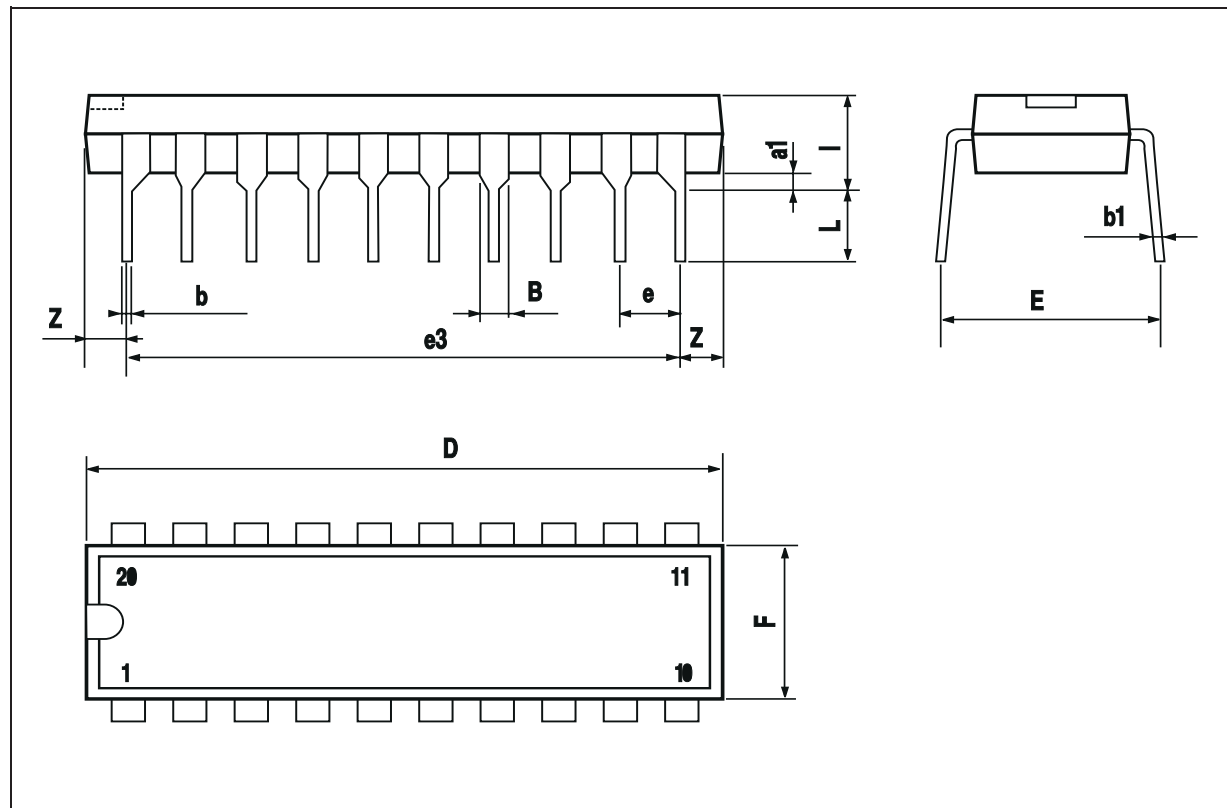
30W	+50W	+90W	+130W
BDW 93/94A	BDW 93/94B	BDV 64/65B	MJ 11013/11014

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

**OUTLINE AND MECHANICAL DATA**



**DIP20**



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